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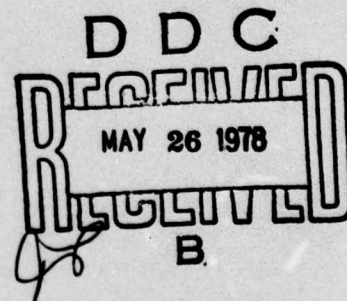
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APPROVED:

Fred Wilson

FRED WILSON
Project Engineer
Intelligence Systems Section

APPROVED:

Howard Davis

HOWARD DAVIS
Technical Director
Intelligence & Reconnaissance Division

FOR THE COMMANDER:

John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

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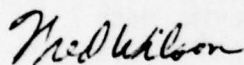
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EVALUATION

This final technical report presents a summary of work performed by Harris Corporation Electronic Systems Division under Contract F30602-76-C-0445. The objectives of this effort was to develop a security monitoring subsystem for the AN/GYQ-21(V) Interactive Analysis System (IAS). The approach of this initial study effort was to evaluate technical feasibility and develop detailed specifications for prototype fabrication. The significance of this effort in relation to Air Force technical objectives is that the report finds that with recent advancements in microcomputer technology it is technically feasible to achieve security in computer systems and recommends an engineering model that would confirm the findings.



FRED WILSON
Project Engineer

1.0 SUMMARY

1.1 Purpose. The purpose of the "Intelligence Security Subsystem" study was to find ways of protecting data in the Interactive Analyst Console, the AN/GYQ-21(V).

1.2 Technical Problem. Access to classified documents is controlled by a system of locks, safes, vaults, protective facilities, cleared employees and security personnel. Access controls to protect the data stored in computers are complex hardware/software mechanisms. Vulnerability tests described in Section 3 of the report have proven these controls to be ineffective. The controlled data, function, equipment, and uses differ considerably in application of automated intelligence systems as used by the Defense Intelligence Agency, the Unified and Specified Commands, and the Services. Section 2 of the report describes some of the applications and presents the conclusion that a simple model incorporates the essential features of access control problems in most applications.

In this model the data requiring data control access resides on disk file and is organized in the form of records, messages, reports, journals and other forms. Data is assumed to be organized into variable length records for simplicity. Each record is assigned a security level, intelligence compartment and "need to know" category. The term "intelligence compartment" is defined as the privileges required to access a record. It is convenient, though inaccurate, to think of the data base as comprising a number of mutually exclusive compartments, each containing a number of records with the same privileges required of a user to access those records - much of the library might be separated into isolated compartments, each containing a number of books. Essentially, the user control problem is to allow access to all authorized compartments and to prohibit access to all other compartments.

1.3 General Methodology. The ideal method of estimating protection afforded by a particular computer architecture would be to build a system and invite the world's leading computer crime experts to try and steal data. The time it would take to accomplish the espionage would be a measure of the protection afforded by that computer.

Obviously, such a method would be both time consuming and expensive. Performance requirements would set the minimum penetration time at somewhere in the range of a decade to a century. Exhaustively testing the hypothesis the minimum penetration time of 10 years, would be out of the question. Still, penetration teams provide a valuable service. Their tactics must be understood before computer systems can be designed, much as safe-cracking tactics must be understood by vault designers.

The method of evaluating alternative computer architecture used in this study is to assume the criminal has gained access to the terminal, and is both highly trained and talented in employing the most effective

penetration tactics. The figure or method for a particular architecture is the estimated penetration time. Comparisons of alternative computer architectures is then accomplished by examining the penetration time estimates.

1.4 Technical Requirements. The specification for a secure data base system is contained in Section 9 of the report. It calls for the design of a secure data base system prototype utilizing enciphering techniques to control access to the data.

2.0 CONCLUSION

The results of the study demonstrate that it is feasible to protect data. The most effective means is to encipher the data base and control access by exit guards at the terminal.

- Database Guard - The Database Guard approach allocates one central processing unit for each security compartment. Upon completion of the sign-in procedure, the user is switched to the computer that corresponds to the user's access privilege. A Secret privilege user will be switched to a Secret computer and will be denied access to Top Secret records in this computer. Potential vulnerabilities are the database guard (multiported disk controller) and the initial switching mechanism. Design of the database guard is presented in Section 7. It was shown that the microprocessor that controls communication into and out of the database has a small program that can be certified. This will prevent the insertion of trapdoors that would defeat the protection mechanism. The initial switching mechanism transfers the Secret user to the Secret IAS. It also represents a potential vulnerability. If the mechanism can be tricked into switching the Secret user to the Top Secret machine, the protection mechanism can be defeated. Fortunately, the microprocessor that performs the initial switching function has a small program that can be certified. We conclude that the potential vulnerabilities can be made impenetrable and as a result, the data base guard approach can be used as a basis to develop a secure IAS.
- Enciphered Record - The Enciphered Record approach presumes the processor is a hostile environment and applies the principles of RED/BLACK isolation the same as used in telecommunications. The records of the data base are enciphered, and even if accessed are useless without the ability to decipher them. The approach has appeal in that it is an elegant engineering solution to the problem of protecting data. Potential vulnerabilities of the system consist of: the access control mechanism, RED processor, cracking the code, and stealing the key. The access control mechanism, like that of the data base guard, is comprised of a small microprocessor with certifiable software. Alternatively, the whole mechanism may be hardwired, thereby, eliminating the software problem. The problem of isolating the RED processor was addressed in Section 7 with the conclusion that the BLACK processor can be totally isolated from the RED processor. We have assumed throughout that a block enciphering algorithm will be used that is impenetrable. For the initial design purposes, the NBS algorithm will be used, although it is recognized that this is unacceptable for military applications. We assume the Government will supply a military-acceptable block encryption algorithm. The final way the system is defeated

is by stealing the key. This can be made impossible by a number of means. One way is to manually insert the key at the guard and design the guard in such a way that if a penetration is attempted the guard will destroy the key before anyone can gain access to it. The sections on RED/BLACK multiprocessing and the enciphered data base system were intended to demonstrate the complexity of making this approach invulnerable. On the basis of information set forth in the report we conclude that the potential vulnerabilities of the enciphered record approach can be made impenetrable and, therefore, the enciphered record can be used as a basis for developing an impenetrable IAS.

- Tag Approach - The Tag Approach to record security utilizes an enciphered tag to inform the exit guard of record classification. The approach is the simplest of the three and only requires an access control mechanism. Since the records are in the clear, RED/BLACK multiprocessing is not required. The approach is an effective measure against the threat of accidental disclosure. For this threat, it is the cheapest and will do the job. We, therefore, conclude that this approach is optimum against a benign threat. On the ability to withstand the attack by computer criminals, we are much less confident. As in the case of the enciphered record, potential vulnerabilities are: access control mechanism, cracking the code, and stealing the key. But unlike the enciphered record approach with the data and records in the clear, the tag approach utilizes records that are in the clear. Therefore, they can be copied and dumped on a terminal or disguised as an error message and sent to the user. There are counter-measures to this vulnerability such as placing an exit guard at every terminal device and designing nonrecord communication containing an unforgeable tag, that describes the transaction as such. In practice, these may or may not be easy to implement. There is some doubt and, therefore, we do not recommend a tag approach against the threat of malicious attack at this time.

3.0 RECOMMENDATIONS

Since, of the three possible approaches, one is at least questionable in its ability to withstand criminal attack, there remains only two possible alternatives for recommendation in its use in development of an engineering model. The data base guard approach appears the least vulnerable, but it is the most expensive. We, therefore, do not recommend it for implementation. There is a second reason for this. There is very little question of feasibility and building an engineering model of the data base guard approach would prove very little. Accordingly, we recommend that an engineering model of the enciphered record approach be developed as specified in Section 9 of the report. Some experts will undoubtedly argue that building an admittedly special purpose data base system is not as productive an area of research as approaches to general purpose solutions, such as on-going efforts to develop secure operating systems. Harris disagrees. First of all, a secure data base system would satisfy many military needs, not only in the intelligence community but also in command and control. Secondly, building special purpose machinery is an inductive approach to the general purpose problem. We have already observed that RED/BLACK multiprocessing is necessary to solve the secure data base problem. Quite possibly, a more general multiprocessing architecture will provide a basis for a multilevel secure computing system.

4.0 IMPLICATIONS FOR FURTHER RESEARCH

Harris Electronic Systems Division recommends that the Government continue the research by implementing the prototype as specified in Section 9 of the report.

SECTION 1.0
INTRODUCTION

1.0 INTRODUCTION

Electronics has made advances in the collection, distribution, and production of intelligence possible. Recently, the availability of data base teleprocessing systems permitted automation of certain intelligence functions with attendant advantages of rapidly correlating information.

Unfortunately, computers suffer from a serious performance deficiency - they cannot protect data. This flaw is fatal in intelligence applications where no threat of espionage can be tolerated.

Despite the inability of computing machines to control data sharing, certain restricted applications are being developed. The restriction pertains to the users in that each (user) must be cleared to receive any and all information from the data base. Not only must the user have security clearances corresponding to the highest level of data contained in the computer, but must also be allowed access to all intelligence compartments.

In practice, this restriction limits the exploitation of automated data base systems. The proliferation of "high water" systems would destroy the information protection afforded by compartmentalization.

The purpose of this study is to find ways to improve the protection of data in the Interactive Analysis System, AN/GYQ-21(V), which is used extensively to automate intelligence and command control functions.

1.1 The Problem of Data Protection. Access to classified documents is controlled by a system of locks, safes, vaults, protected facilities, as well as cleared employees and security personnel. Access controls to protect data stored in computers are complex hardware/software mechanisms. Vulnerability tests, described in Chapter 3, have proven these controls to be ineffective.

The controlled data, function, equipment, and uses differ considerably in the application of automated intelligence systems as used by the Defense Intelligence Agency, the Unified and Specified Commands, and the services. Chapter 2 describes some of these applications and presents the conclusion that a simple model incorporates the essential features of the access control problems in most applications.

In this model, the data requiring controlled access resides on a disk file and is organized in the form of records, messages, reports, journals, and other forms. Data is assumed to be organized into variable length records for simplicity. Each record is assigned a security level, intelligence compartment, and "need to know" category. The term "intelligence compartment" is defined as the privilege required to access a record. It is convenient, though inaccurate, to think of the data base as comprising a number of mutually exclusive compartments, each containing a number of records with the same privilege required of a user to access

those records - much as a library might be separated into isolated compartments, each containing a number of books.

Essentially, the user control problem is to allow access to all authorized compartments and prohibit access to all other compartments.

1.2 Scope. An electronic record access control system can be defeated in a number of ways. Most are considered in Chapter 3, "Threat Analysis." However, three threats that have well understood countermeasures utilizing technology significantly different from that considered in this report are specifically excluded from consideration in this study. These threats are:

- Masquerading - Each user must identify himself when signing on the computer. Next, the user must validate identity, usually by typing in a password. This method of identity verification is vulnerable. Improved methods based upon fingerprints, voice prints, hand geometry, signature, and others are being explored; not only to improve computer security, but for commercial, industrial, and residential security applications as well.
- Wiretapping - A user with low access privilege may tap lines of a user with higher access privilege thereby gaining unauthorized access. This can be, and is frequently, prevented by enciphering data or by security guard surveillance.
- Monitoring emanations - Data communication and processing within the computer results in emanations which can be monitored by instruments. Vaults, shields, isolation components, and other means of control are commonly employed.

In addition to the three threats, one approach is also excluded from consideration.

- Secure software - The problem of access control would be solved, by definition, if secure software were available. Specifically, efforts have been made to develop a kernel for the PDP-11/45 which could be adopted for compatibility with RSX-11D utilized in the AN/GYQ-21(V). Efforts to develop secure software, unfortunately, have not succeeded to date. For example: the Air Force Electronic Systems Division abandoned efforts in this area after 6 years and several millions of dollars in expenditures. The bibliography of reports issued upon termination of similar activities identifies 76 studies. The consensus is that this study is unlikely to succeed where those had failed. IBM announced a \$40 million program on computer security some years ago. Their current view¹ is that development of a secure operating system is beyond the state of the art.

¹As expressed by Mr. Courtney, IBM Manager of Computer Security at the annual Computer Security Institute meeting in New York City, November 1976.

The decision to exclude secure software from consideration carries with it the implied decision to abandon internal access control mechanisms as these are predicted upon software. Accordingly, the scope of solutions considered is confined to external access control mechanisms. This approach is believed to be a fruitful field of exploration because of the rapid technological advance as evidenced by the microprocessor, enciphering devices on a chip and the rapid and general decline of hardware and firmware prices.

1.3 Method. The ideal method of estimating the protection afforded by a particular computer architecture would be to build the system and invite the world's leading computer crime experts to try and steal data. The time it would take to accomplish the espionage would be a measure of the protection afforded by that computer.

Obviously, such a method would be both time consuming and expensive. Performance requirements would set the minimum penetration time at somewhere in the range of a decade to a century. Exhaustively testing the hypothesis that the minimum penetration time is 10 years, would be out of the question. Still, penetration teams provide a valuable service. Their tactics must be understood before computer systems can be designed, much as safecracking tactics must be understood by vault designers.

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1.4 Tactics of Computer Criminals. Recorded and postulated criminal tactics are many and varied, involving attacks by maintenance, operations, and development personnel (alone and in conspiracy). In essence, all espionage attacks proceed in two steps: first, the criminal gains command of the system; and then dumps the protected data.

To understand the specifics of the tactics, suppose a criminal somehow gained the privilege of reading or writing any word in the computer's main memory. The criminal could then proceed with any or all of the following tactics:

- Dumping the password file - This tactic may, and frequently is, countered by enciphering the passwords. Still, a criminal can get all users' passwords if clear text copies can be obtained. These passwords can then be used to masquerade as a user with higher privileges.
- Falsifying the access control list - When a new user signs on a typical system, the user's Social Security number must be supplied as a means of identification (ID). The computer checks the Social Security number and finds the access privileges for that particular

user. (The list of users and their access privileges are contained in the access control list.) If a malicious user is free to read and write information on core storage, access privileges can be falsified.

- Masquerading as a user with higher privilege - A related technique falsifies an ID held by the computer system to identify the current user in a time-sharing system. For example: if the ID is falsified, the malicious user can masquerade as the system administrator with access privileges to all parts of the system.
- Commanding the operating system to dump privileged data - If the user is allowed to read and write into any access location, it is possible to modify and, therefore, command operating system modules. All the operating systems - RSX-11D, GECOS III, etc., - are in the public domain. Copies of the listings can be readily obtained. An accomplished criminal can find the location of the operating systems in core memory and modify them as desired. For example: a data base retrieval module can be modified to dump any records contained in the data base. While there may be some difficulties encountered in reading the octal codes and in locating the modules in memory, these problems are not insurmountable and could certainly be accomplished within a few days.
- Writing and executing programs that dump any information in the data base - It has been sometimes naively assumed that, by eliminating the programming capability of the user or by eliminating or protecting the operating system, a penetrator could not gain unauthorized access. Such is not the case. Even if the system has no operating system modules to command, the user can create such modules by programming in machine language. Such an approach is awkward and more difficult than programming in assembly or higher level language, but it is certainly well within the realm of feasibility.

The preceding list is by no means complete, but it will serve to illustrate tactics that can be effective for an espionage agent.

The criminal can also crash the system by writing into the operating system and by other means. Such a sabotage attack is not, in our view, considered serious because service would only be denied for a brief period of time. For example: in the National Military Intelligence Center (NMIC), copies of the operating system are available on-line and can be reloaded in a matter of minutes. The criminal might persist by attempting to crash the system several times which would be extremely dangerous for him. For this reason, the study does not consider the problem of preventing a sabotage attack. Indeed, this is thought to be improbable.

The conclusion is inescapable - if there is any way the criminal can gain the power to read and write any one word in main memory, the penetration time to unauthorized data will be minutes, or even seconds; rather than decades as prescribed by required performance.

Chapter 3 provides details on how the criminal can gain the ability to read or write any word in computer main memory. The category of tactics is summarized as follows:

- Trap door attack - The simplest way for the malicious user to gain control over the system is by use of what's termed a "trap door" that can be inserted by an accomplice in minutes. The trap door may be as small as one or two instructions and is almost impossible to detect. It is like looking for a needle in a haystack to find two instructions in tens of thousands.
- Exploiting software flaws - While the insertion of a trap door is a rather simple task, the RSX-11D operating system is developed without security controls and maintenance programs are communicated in an unclassified form. Even so, it is still unnecessary for the penetrator to rely on trap doors. A flaw in the software will give the criminal the needed capability to read and write an arbitrary word in main memory. Examples are detailed in the body of this report.
- Exploiting hardware flaws - That numerous software flaws exist in RSX-11D is certainly the case. One example is given in the body of the text. Even if this is not the case, there are probably hardware flaws in the PDP 11/45 that could be exploited. Examples of how such a hardware flaw was found in the MULTICS system are given in the body of the report.

1.5 Evaluation of Candidate Architectures. The analysis documented in Chapter 3 estimates the time it would take a competent criminal to gain unauthorized access to one or more records stored in the data base. Penetration time estimates are compared for a number of candidate protection methods. Comparison of alternative approaches, i.e., architectures, is based upon two criteria. First, espionage must be impossible for all practical purposes, i.e., penetration time estimates must be years, if not decades, to access a single record. Second, the solution should be affordable, i.e., the total incremental cost including hardware and software modifications should be less than the cost of alternatives. The engineering problem is one of selecting an approach that has an acceptable performance (penetration time) and a minimum cost.

The variation in cost and performance among candidate computer architectures is so pronounced that sophisticated analysis is not required in most cases. Seven of the ten candidates examined totally failed to prevent espionage. Of the remaining three, a serious question about the performance of one candidate exists. Deciding between the remaining two requires detailed preliminary design.

Highlights of the Chapter 4 analysis are summarized below.

- Existing AN/GYQ-21(V) - Harris ESD penetrated the IAS² in 2 hours in an experiment conducted as part of the study. Undoubtedly, many exploitable flaws exist in both RSX-11D, the application software, and the PDP-11 hardware. No attempt at identification was made since their existence is academic. A trap door that would allow any terminal user total access to the system in a matter of minutes could easily be inserted.
No consideration should be given to compartmentalize security using the IAS. Denying programming access to terminal users is an ineffective procedure since the trap door provides programming access, although only in machine language.
- Security monitors - It is considered conventional wisdom to monitor interactive dialogue for the purpose of detecting computer crime, much as some banks continuously photograph their lobbies to obtain evidence when a crime occurs. The analogy is a bad one because espionage can be completed without producing a detectable audit trail.
For example: A terminal user could type in a character sequence such as "ZYQMG" that would trigger a trap door to dump certain unauthorized information at the penetrator's terminal. Logs of the traffic both into and out of the data base would provide no clue that unauthorized data had been requested or that the request had been honored.
Bypassing security monitors embedded in existing systems is even simpler. Even if incriminating information is collected, the espionage agent can simply write and read the logs so as to erase any incriminating information. In one way, security monitors are worse than useless because they seem to provide a measure of insurance, yet are totally ineffective against a competent computer criminal.
- Isolated security monitors - It is entirely possible to build micro-processors or minicomputers that are totally divorced from the main computing system and record interactive traffic. Logging functions are relatively simple, so the software can be held to a minimum. This can be certified, and assurances against the penetrator falsifying the logs can be made. Still, this approach cannot deal with the problem of interpreting stimulus and response, cited above. Accordingly, we also view isolated security monitors as ineffective with one important exception: While security monitors by themselves will not preclude the possibility of espionage, they can be an effective aid when used in conjunction with other methods.

²Interactive Analysis Station (IAS) is another name for the AN/GYQ-21(V).

- Entrance guards - As the name implies, the concept involves placing automated devices to monitor the user input portion of the dialogue. Unlike security monitors, entrance guards operate in real time. When authorized access is detected, the Access Control Center (ACC) is notified. The security officer, resident at the ACC, is notified of the anomaly and takes preventive action. Entrance guards have the same fatal flaws of isolated security monitors - They cannot detect attempted espionage by an accomplished computer criminal with 100 percent accuracy.
- Exit guards controlling access to enciphered records - This approach requires a radically different architecture. The data base system comprises a number of variable length records that are all enciphered. Assuming that the espionage agent can freely access the records and that the information is protected by the enciphering process, theory is that the criminal cannot crack the code in any reasonable period of time without a code key. Harris ESD believes such an approach has merit because it is capable of satisfying the penetration time requirements. In addition, this architecture does not appear to have a serious cost penalty because of inexpensive hardware availability for encryption and decryption. Feasibility is a far more serious question. At some point in the computer, operations must be performed on the records in all the data base applications that Harris ESD studied. For example: In the National Military Intelligence Centers, incoming messages are read by the computer to determine distribution of message copies. Obviously, no reading can take place if the records are enciphered. The problem can be circumvented by having two processors totally isolated from each other. The first, called the "black processor," always contains enciphered records. It is assumed that the criminal can freely access any of those records, but is denied the information content due to lack of an enciphering key. The second processor, called the "red processor," receives records from the first processor; and deciphers, processes, reenciphers, and returns the messages to the black processor. RED-BLACK isolation is adhered to in the two processors much as they are in standard communications equipment. The problem with this approach is that RED-BLACK isolation must be achieved. The danger is that a secure multiprocessing system (RED-BLACK processors) is similar to the isolation of multiprogramming capability which has defied solution for the past decade. This turns out not to be the case. Results of analyses in Chapter 6 are positive that RED-BLACK isolation can be achieved.
- Exit guards operating on control tags - The problem of secure multiprocessing can be bypassed if, instead of enciphering the entire message, only a tag is enciphered. The tag contains a nonforgeable compartment identification. The methods of preventing forgery are critical to the estimates of penetration time presented in Chapter 4. In summary, it is felt that the time to forge a tag can be maintained to an arbitrary long period provided a sufficiently sophisticated algorithm for enciphering the record and computing parity bits is maintained.

The control tag approach requires additional equipment. An exit guard must be placed between each terminal in the system, or one guard must be multiplexed among the number of terminals. An access control center must be available to identify the user and pass access rights to the exit guard. Further, all incoming messages must be tagged in order for the system to work effectively.

Preliminary cost estimates indicate that this would amount to an incremental cost of perhaps 1 to 3 percent of the hardware and software costs of a large data base system. Harris ESD does not feel such a cost prohibitive, but no general statements should be made. Judgments should be made on an application-by-application basis.

A severe problem with the tag approach is that of preventing a malicious user from bypassing the exit guard. Results of analysis are inconclusive on this point.

- Data base guards - A positive method of controlling access to the data base is to allocate one IAS for each security compartment and control access from the data base to that computer through a multiported memory. In that way, the compartment identification contained in each record is examined by the multiported memory after the request has been honored. If the addressed computer does not have the required access rights, the multiported controller denies the request and notifies the access control center. While this architecture appears to be unpenetrable in any period of time, it does have an associated serious cost problem. If, for example, a half dozen intelligence compartments and two levels of security with several need-to-know restrictions are involved, the computer count could run to over a dozen. If, however, the data base had no need-to-know restrictions, was all of the same security level, and had only two compartments; only two computers would solve the problem. Multiple computers are not as serious a problem with the IAS because they represent a relatively small amount of the total system cost - small, relative to the data base and other peripherals. Still, this architecture is the most expensive.

1.6 Conclusions and Recommendations. The most important conclusion of the study is that it is feasible to design a secure data base system. This conclusion is based upon the findings of the data base guard approach and enciphered record and presupposes that the design of the data base guard, the multiported memory, would have a modest amount of software programs sufficiently small so that they could be certified. Such appears to be the case.

The conservative recommendation would be to go ahead with the design of the data base guard approach because there is a high probability that no penetration team would be able to gain unauthorized information. It is also likely that theoretical arguments could be developed to show that no unauthorized information could be obtained in any reasonable period of time and sufficient evidence provided to the Government to allow certification of the data base approach. While such a recommendation would assure the

demonstration feasibility, it would introduce a cost problem. The necessity for multiple computers and the associated core memory would preclude the retrofitting of existing systems.

An additional reason for not recommending demonstration of the data base guard architecture is that little (or no) questions of feasibility exist. Multiported memories are well understood, have been built by Harris ESD and others, and are well within the state of the art. Building such a system would prove little or nothing.

Accordingly, the choice of alternative architectures to implement is narrowed to two.

- The clear record enciphered tag - This approach may or may not work. While it seems apparent that all but the most gifted criminals could be prevented from accessing unauthorized information, there is always the danger of some innovative tactic succeeding, such as bypassing exit guards, bribing or subverting maintenance personnel, and utilizing administrative traffic communication to convey information. This study reaches no conclusion as to whether the clear record/enciphered tag approach will guarantee that a user cannot access unauthorized information. Some progress has been made in assessing the details necessary to implement a dedicated, or retrofit, an IAS system. More work is needed. Because there is some doubt about the performance of this approach, it is not recommended for future development.
- Enciphered records - This second alternative has the appeal that - even though the computer environment may be viewed as hostile and users are exploiting flaws, trap doors, subversion of maintenance personnel, etc., - the computer criminal is denied access to the information although the enciphered data is freely accessible. From an engineering point of view, this approach is conceptually elegant. The problem of defining how, isolation of RED-BLACK processors can be achieved has been accomplished. On this matter, the current study is positive. This leads to the recommendation that the design and implementation of the enciphered record approach also be pursued.

1.7 Compliance With the Statement of Work. The remaining portion of this report is organized into eight sections as described in the following paragraphs. The presentation is intended to conform to contractual requirements as set forth in the research and technology work statement.

Section 2, Background on the AN/GYQ-21(V), complies with Section 2 of the work statement. "The scope and proposed study is the IAS security protection in environments at HQ SAC, ADCOM and DIA" presents the description of the hardware and software of the IAS as well as its use in intelligence application.

Section 3, The Threat, complies with Paragraph 4.1.1.3 of the work statement. "Develop a strategy and tactics of malicious users. This task shall catalog ways of penetrating the IAS."

Section 4, Evaluation of Candidate Approaches, complies with Paragraph 4.1.1 of the work statement. "Examine various hardware/software approaches against actual security requirements and to recommend viable solutions using microprocessor technology. The security subsystem shall be an external control mechanism utilizing microprocesses."

Paragraph 4.2 of Section 4, Entrance Guards, complies with work statement Paragraph 4.1.1.4. "Examine the allowable sentence structures which may be composed by various users. The examination shall be utilized to build the query parameters allowable by operational intelligence analysts using the microprocessor."

Section 5, An Experimental, Enciphered, Data Base System, deals with two of the most promising approaches, the enciphered tag and the enciphered record. It is intended to comply with three sections of the work statement described as follows:

- Paragraph 4.1.1, "Design a Monitory and Control Unit that will prevent any accidental release of messages."
- Paragraph 4.1.1.2, "Design a Monitory and Control Unit that will prevent malicious users from damaging or compromising intelligence information in the AN/GYQ-21(V)."
- Paragraph 4.1.1.5, "The contractor shall design a malicious user protection mechanism and perform the synthesis over the detection algorithm and appropriate devices."

Section 6 of the report, RED-BLACK Processing, treats the problem of isolating the black processor from the red processor which has the capability of deciphering the records. It is a critical problem in the utilization of the enciphered record approach.

Section 7, Data Base Guard Approach, treats in some depth the problem of designing and developing a multiported memory for the multiprocessing configuration to achieve compartmentalized security.

Section 8, Findings, Conclusions and Recommendations, presents the results of the study.

Section 9, Specification and Security Monitoring subsystem complies with two sections of the research and technology work statement. Section 1, "The objective of the proposed program is to develop a security monitoring subsystem for the AN/GYQ-21(V) interactive analysis system (IAS). This initial effort is a study of evaluating the technical feasibility and development of the detailed specification of the prototype fabrication."

This chapter also complies with Paragraph 4.1.2, "Develop the Final Design for the Microprocessor. It shall consider the tasks of Paragraph 4.1.1 and based upon these tasks shall select an optimum approach based upon performance, cost and requirements."

SECTION 2.0

AN/GYQ-21(V) BACKGROUND

2.0 AN/GYQ-21(V) BACKGROUND

Scope of this study is limited to "Interactive Analysis Station (IAS) security protection in environments of Headquarters Strategic Air Command (HQ SAC), Aerospace Defense Command (AECOM), and the Defense Intelligence Agency (DIA)." This narrows the consideration of hardware, software and applications.

The central processing unit discussed in Paragraph 2.1 is limited to the Digital Equipment Corporation's PDP-11 series computers. Models 11/45 and 11/70 are in use in AN/GYQ-21(V) applications. The 11/60's are planned and undoubtedly others will be employed as they are announced. The PDP-11 product line is a dynamic one which is almost a decade old with continuing announcements of improved products.

The IAS also utilizes standard software. Up until now the RSX-11D, one of several operating systems developed and commercially marketed by the Digital Equipment Corporation is used in the IAS. Like all operating systems, RSX-11D is both large and vulnerable to penetration. It is discussed in Paragraph 2.2.

The applications of the PDP-11 to military problems are many and varied. It is extensively used in intelligence: it is a standard for the World-Wide Military Command and Control System; it is used for telecommunications, instrumentation, weapons control, scientific research, business data processing and many other applications. The scope of the study specifically limits the consideration of applications to those at the Defense Intelligence Agency, the Aerospace Defense Command and HQ SAC. These are described in Paragraph 2.3.

Paragraph 2.4 describes a typical configuration which incorporates the hardware/software and applications described in the preceding section. It is concluded that a data base system incorporates all the features of the intelligence applications, both existing and planned.

2.1 PDP-11/45. The source of information on the IAS hardware central processing unit is contained in the booklet entitled, "PDP-11/45 Processor Handbook" published by the Digital Equipment Corporation, Maynard, Massachusetts. Other models of the PDP-11 used in the IAS are essentially similar to the PDP-11/45. Chapter 6, Memory Management, describes the controls. In essence, there are three states in the IAS, each having different privileges. There are user states which may be occupied by several different users, each having different memory access privileges. There is a supervisory state, and, finally, the kernel state. The kernel state is the most privileged and freely accessed and controls all information.

Table 1 describes the capabilities of the three states. The user state is limited in the area of memory it can address. The limitation is a specific number of virtual pages. Further, the user state is prohibited from exercising certain instructions, among them are input/output instructions, instructions assigning memory bounds, and instructions to change the state.

TABLE 1. IAS STATE CAPABILITIES

Mode	Ability To Address Memory	Instructions Prohibited	Trap, Abort Or Interrupt
User	Limited to assigned pages	Input/output Assign memory bounds Change state	Transfer control to kernel state
Supervisory	Limited to assigned pages	Assign memory bounds Change state	
Kernel	No limitation	No limitation	

Further note traps, aborts, or interrupts usually result in transition to the kernel state.

The supervisory state is also limited to assigned pages, but it can execute input/output instructions. It cannot change state or assign memory bounds. The kernel state has unlimited access to instructions and memory. It exercises control over the computing process by transferring control to the kernel state after traps, aborts, and interrupts.

The access controls to memory are specified by the access control field (ACF) of the Page Descriptor Register. Table 2 shows the access privileges.

The basic flaw in the hardware control is that if the malicious user can somehow enter the kernel state, all controls are bypassed and the user has free command of the system.

2.2 RSX-11D. The IAS software falls into two categories: the RSX-11D Operating System, and the applications program. The Applications Program runs in the user mode and is not usually exploited by the computer criminal. By contrast, RSX-11D runs in the supervising or kernel mode and is usually the target of attack.

RSX-11D is the standard operating system used with the IAS. Like all operating systems, it exercises executive control over the computing facilities with the object of maximizing throughput via multiprogramming.

TABLE 2. CONTROL ACCESS PRIVILEGES		
Access Code	Mode	Function
000	Nonresident	Abort all accesses
001	Read-only	Abort on write attempt memory management trap on read
010	Read-only	Abort on write attempt
011	Unused	Abort all accesses - reserved for future use
100	Read/write	Memory management trap upon completion of a read or write
101	Read/write	Memory management trap upon completion of a write
110	Read/write	No system trap/abort action
111	Unused	Abort all accesses - reserved for future use

2.2.1 Functions. The principal functions of the IAS operating system are:

- Executive
- System generation
- Input/output operations
- Utilities
- Operating procedures
- Compilers

2.2.2 References. Details on the performance of these functions are contained in the following documents:

- Introduction to RSX-11D
- RSX-11D Concepts and Capabilities
- RSX-11D System Generation Reference Manual
- RSX-11D Input/Output Operations Reference Manual
- RSX-11D Utility Operations
- RSX-11D Operator Procedures
- RSX-11D Task Builder Reference Manual
- RSX-11D On-Line Debugging Techniques
- RSX-11D Device Handler Reference Manual
- RSX-11D Guide to Writing a Device Handling Task
- RSX-11D Macro Assembler Reference Manual
- RSX-11D FORTRAN IV Compiler
- RSX-11D System Test Reference Manual

2.2.3. The RSX-11D Executive. The executive of the operating system has five principal functions as follow:

- Memory management - The Executive is responsible for the allocation of core memory to programs and transfer of programs between core and disk file.
- Control of task execution - Multiprogramming is conducted in a series of tasks, several of which may be simultaneously resident in core memory. The tasks are prohibited from utilizing the input/output equipment or from communicating with each other. These services are performed by the Executive.
- System directories and systems lists - The Executive maintains parameters necessary for operation.
- Control of input/output operations - This critical function performed by the Executive includes controlling the reading and writing of disk files.
- Monitoring the console.

2.2.4 Input/Output Operations. Because the Executive commands the device handlers, and, accordingly, is able to print information out, store, and retrieve it from bulk memory sources, it has the power to bypass all access controls. It is perhaps more accurate to say that the control of input/output operations is, in fact, the access control mechanism. It will be demonstrated subsequently that one of the tactics utilized by the computer criminal is to enter the operating system and create commands for input/output.

2.3 IAS Application at HQ SAC, ADCOM and the DIA. The applications of the IAS are as the name implies controlling traffic to and from intelligence analysts and their terminals. The IAS is an essential link in the communication between man and machine. In general, the IAS is a component of a larger network.

2.3.1 Intelligence Networks. The National Military Intelligence Center is an important application of the IAS because 10 such machines are used and the process is accomplished entirely by the AN/GYQ-21(V). However, there are many other different types of intelligence installations. Figure 1 shows some of the intelligence installations of IAS as used by the Unified and Specified Commands and the Services. The dotted oblong in the center of the diagram encloses all of the computers resident at the Defense Intelligence Agency (DIA). The upper portion of the DIA blocks represent the National Military Intelligence Center.

Outside of the DIA blocks are the installations of the Unified and Specified Commands feeding information into the DIA. At the upper left-hand corner is the Alaskan Command (ALCOM). The lower left-hand corner is the Pacific Command (PACOM) and the center left is the Continental Air Defense Command (ADCOM). The Strategic Air Command (SAC) is shown to the left of the DIA box.

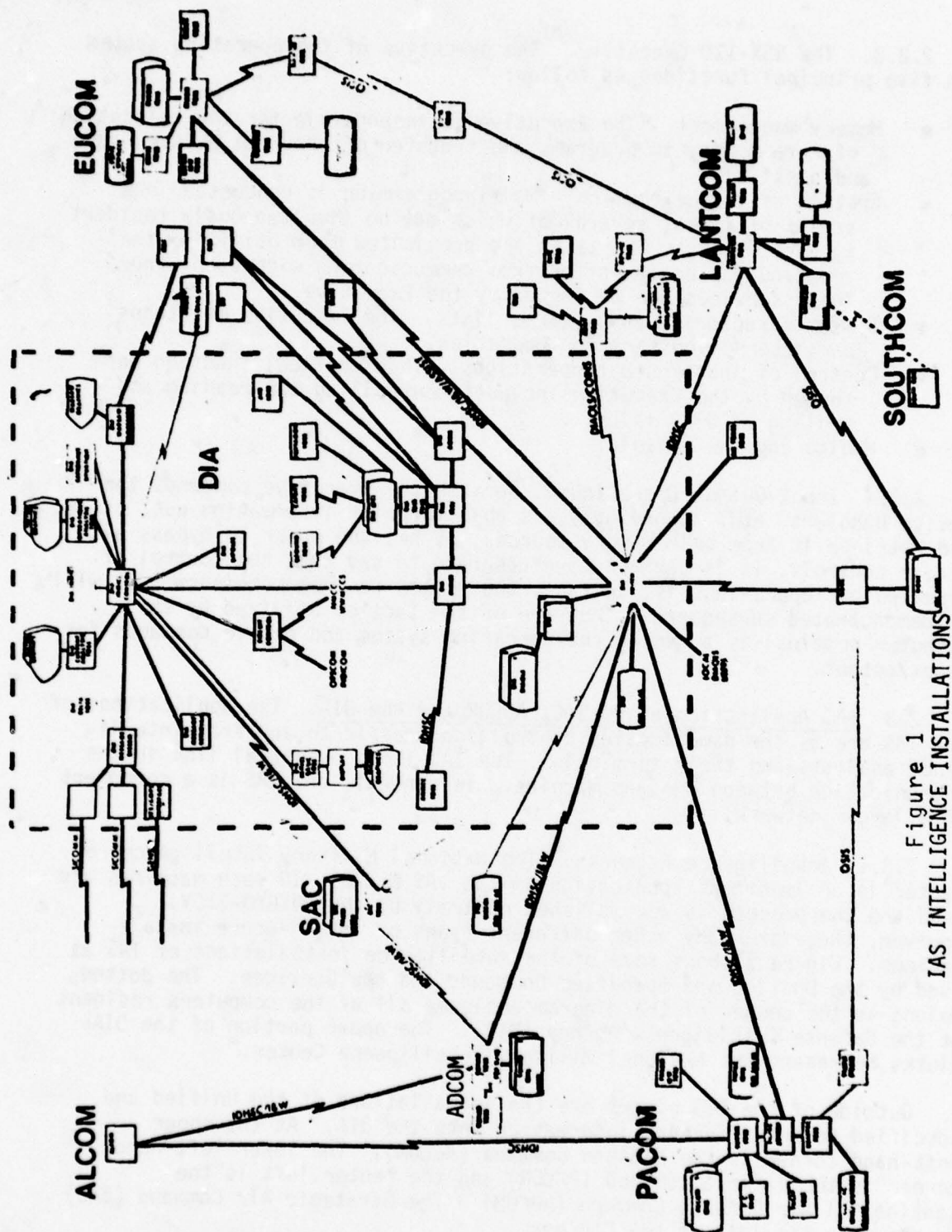


Figure 1
IAS INTELLIGENCE INSTALLATIONS

The upper right-hand corner indicates the equipment configuration at the European Command (EUCOM). And the Atlantic Command is shown on the lower right with a tentative link into the Southern Command.

The major links between the Unified and Specified Commands and the DIA are shown as IDHSC/IW, that is, there are communications links for the Intelligence Data Handling System Communications/Indications and Warning. In some instances the links already exist and are shared by the two applications. Other links are only contemplated.

The intelligence data handling system is comprised of several dozen large computers of various types. A commonly used computer is the Honeywell 600 or 6000 series. Frequently, the IAS is used in conjunction with the larger machines. All IDHS sites contain a large data base associated with the general purpose computers.

The applications of the IAS are twofold: first, there is the stand-alone interactive data base system such as the National Military Intelligence Center (NMIC), shown in the upper center of Figure 1. Secondly, the IAS is used as a communications processor for a large Intelligence Data Handling System, (IDHS) computer.

2.3.2 Stand-Alone, Data Base Systems - NMIC. The focal point in the Pentagon for indications and warnings is the National Military Intelligence Center. NMIC is under development and utilizes 10 AN/GYQ-21(V) computers. The basic function of NMIC is the distribution and recall of incoming messages to intelligence analysts.

Figure 2 shows an overview block diagram of the NMIC support system processors with intercommunications links for normal and failure back up modes. The backup modes are shown as dotted lines. The processors are consecutively numbered 1 through 10 and are arranged in tandem to facilitate failure recovery.

Processors 1, 2, 3, and 4 form the message support subsystem with their supporting peripheral equipment. Principal among these are the data bases. There is a control subsystem shown as the No. 5 Processor which funnels all messages between the users in their origin and destination. The communications processor, INDICOM, is No. 6, and terminates the incoming circuits as well as providing external communications to other intelligence systems. The user support subsystem is comprised of two processors, No. 7 and No. 8, which support the analysts. Half of the analysts are on each of the two processors.

Figure 3 shows Processors No. 1 and 2 with their accompaniment of peripherals. The dissemination analyst bus carries data from Processor No. 1 and interconnects to the following peripherals and memory:

- 120K core memory
- 132 column 1000 line per minute line printer
- LA36-CA teletype

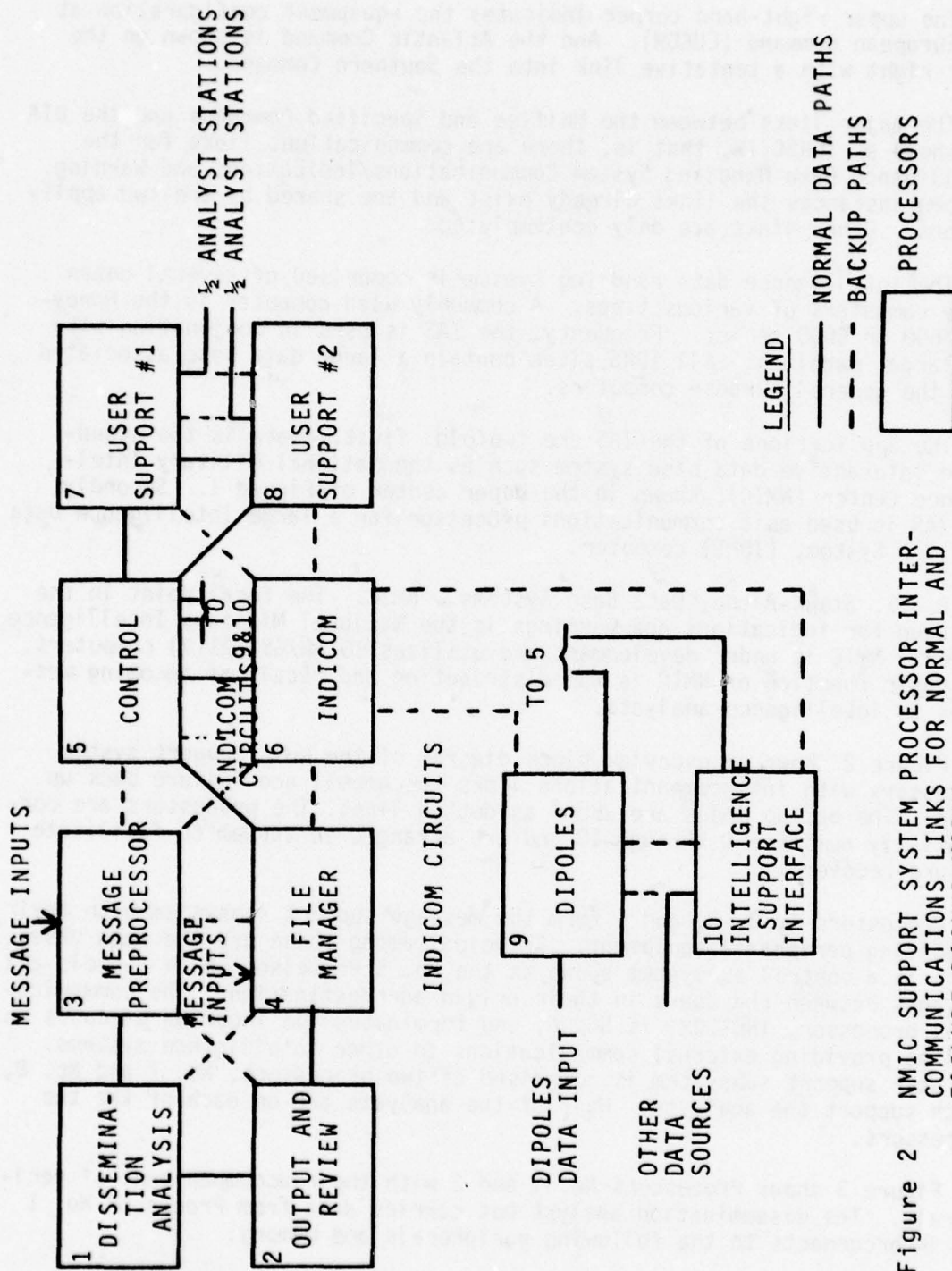


Figure 2 NMIC SUPPORT SYSTEM PROCESSOR INTERCOMMUNICATIONS LINKS FOR NORMAL AND FAILURE BACKUP MODES

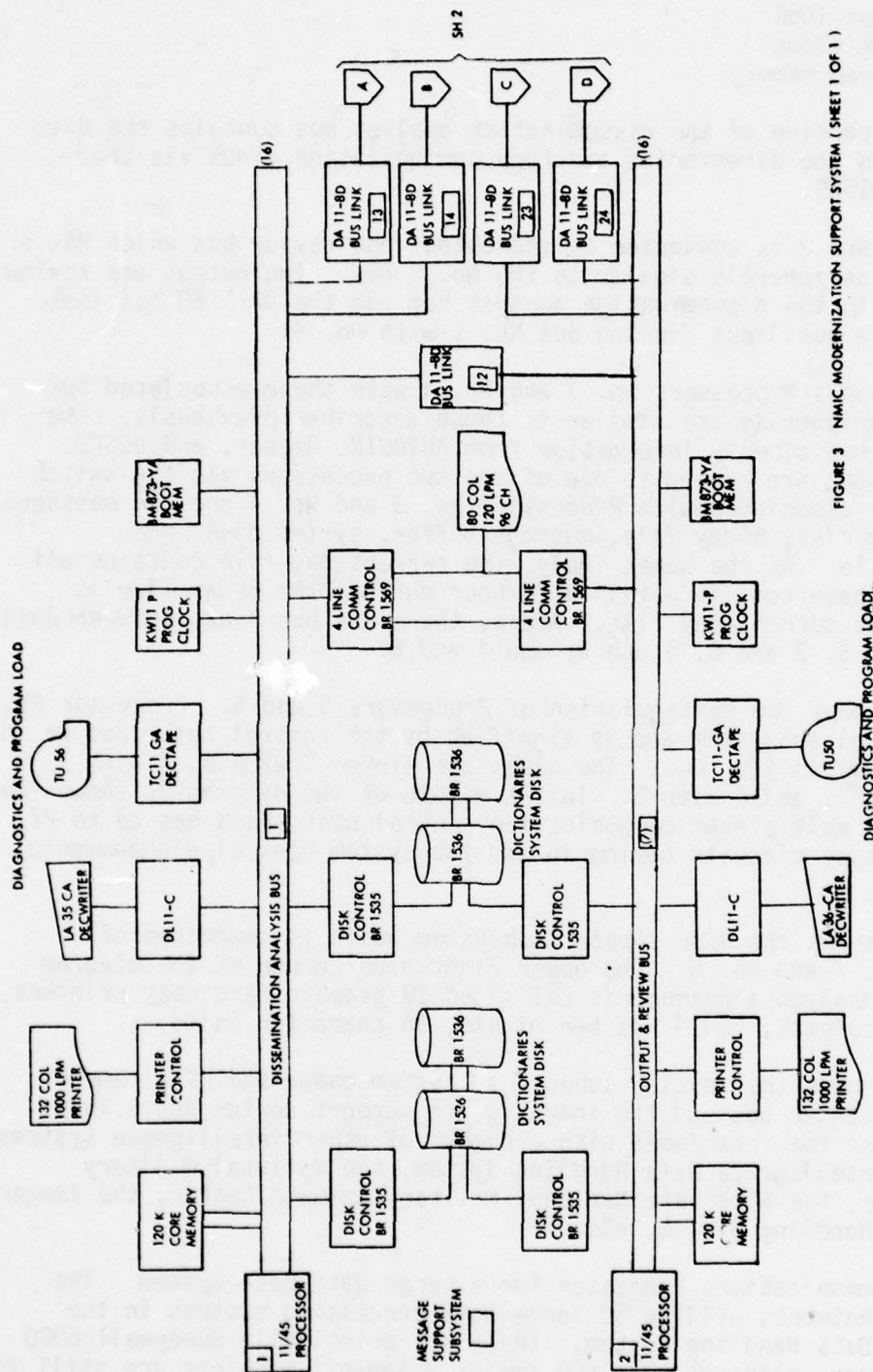


FIGURE 3 NMIC MODERNIZATION SUPPORT SYSTEM (SHEET 1 OF 1)

- DEC tape TU56
- Program clock
- Bootstrap memory

The lower portion of the dissemination analyst bus contains the disk files that hold the directories and four communication lines via the multiplexer BR1569.

Processor No. 2 is connected to the output and review bus which has a complement of peripherals similar to the No. 1 bus. The output and review bus is linked to the dissemination analyst bus via the DA11-BD bus link. Also, there are bus links linking Bus No. 1 with No. 4.

Figure 4 shows Processors No. 3 and No. 4 with their associated bus links. The peripherals are similar to those described previously. The message input bus accepts information from AUTODIN, Genser, and DSSCS. Incoming messages are routed to one of the two processors via the switch. The data bases associated with Processors No. 3 and No. 4 are the message buffer, system disk, 5-day file, message buffer, system disk, and current-day file. As the names imply, the current-day file contains all messages that have come in within a 24-hour period; the 5-day file is archival to the current-day file. Again, there are bus links between Buses 3 and 4, 3 and 5, 3 and 6, 4 and 5, and 4 and 6.

Figure 5 shows the configuration of Processors 5 and 6. Processor No. 5 is the control subsystem and is signified by the control bus. Bus No. 6 is the intercom/profiler bus. The buses are linked 5 with 6, 5 with 7, 5 with 8, 6 with 7, and 6 with 8. In the middle of the diagram is shown the 32 line BR1569 multiplexer communication control unit which has up to 27 INDICOM teletype circuits coming in and two system control alphanumeric CRT's.

Figure 6 shows the user support subsystem which is comprised of Processors No. 7 and No. 8. The upper right-hand corner of the diagram shows the 31 analyst alphanumeric CRT's and 10 graphic hard copy printers, these are 80 columns, 120 lines per minute, 96 character units.

Figure 7 shows the special support subsystem comprised of a remote intelligence center bus and the intelligence support center bus. This system contains the interfaces with a number of other intelligence systems, such as the Intelligence Data Handling System, the National Military Command Center, the Alternate National Military Command Center, the Imagery Related Data Handling System, etc.

2.3.3 Communications Processor for a Large Data Base System. The Intelligence Networks utilize 50 large data processing systems in the Intelligence Data Handling System. These are principally Honeywell 6000 series computers, although some 600 series Honeywell machines are still in use. The typical application of the IAS is to act as a communications processor between these large machines and the user terminals.

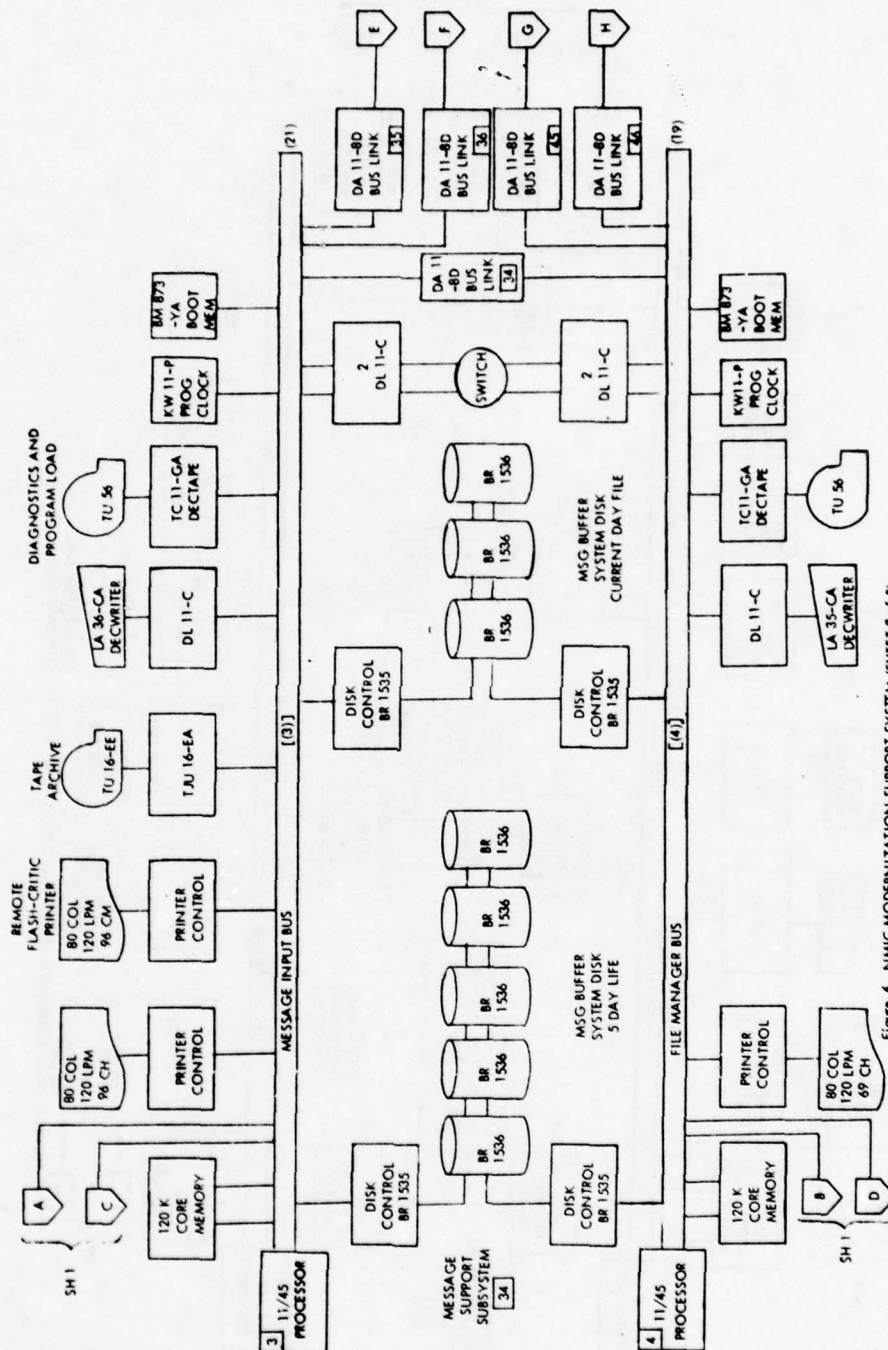


Figure 4 NMIC MODERNIZATION SUPPORT SYSTEM (SHEET 2 of 5)

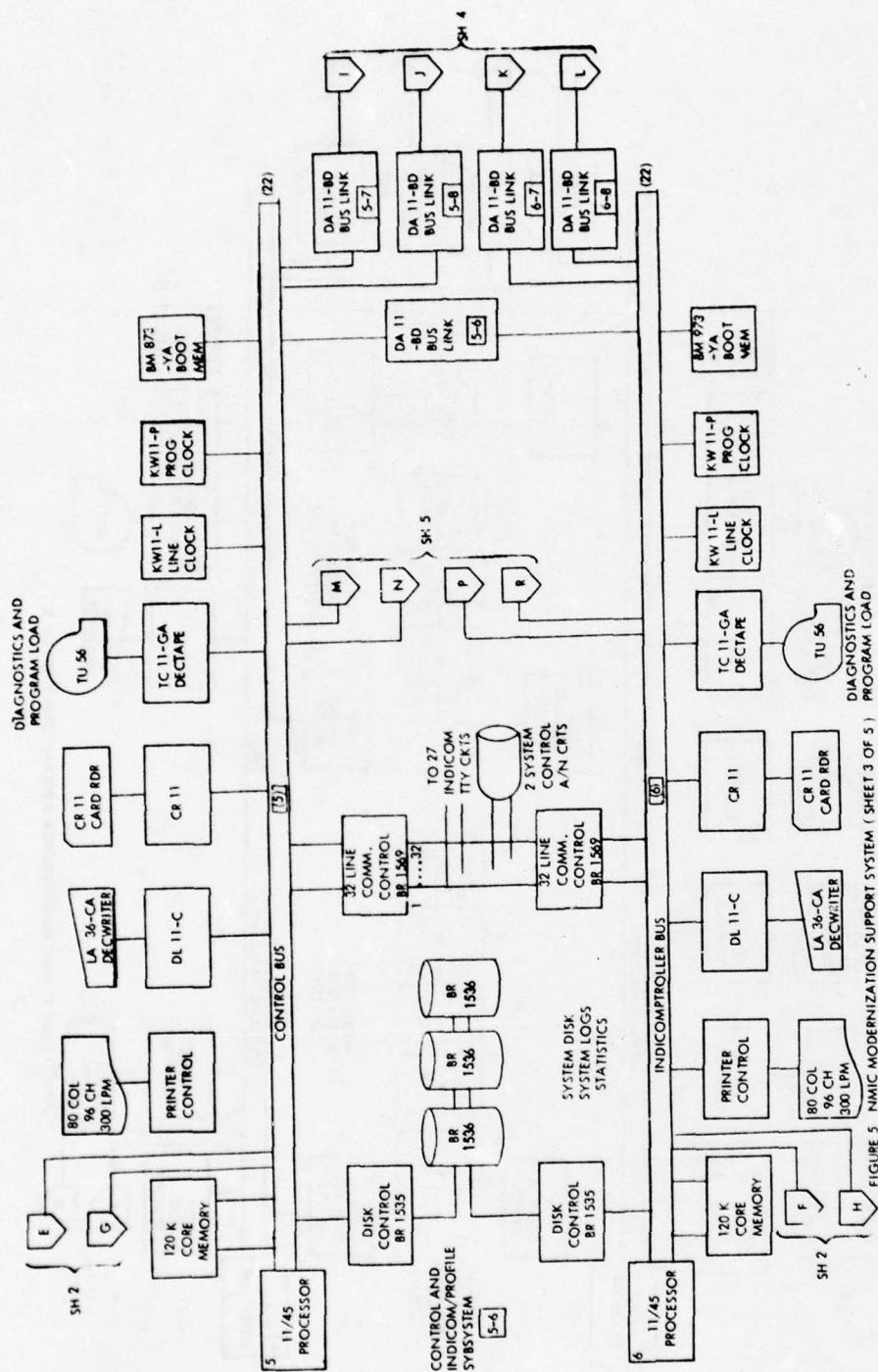


FIGURE 5 NMIC MODERNIZATION SUPPORT SYSTEM (SHEET 3 OF 5)

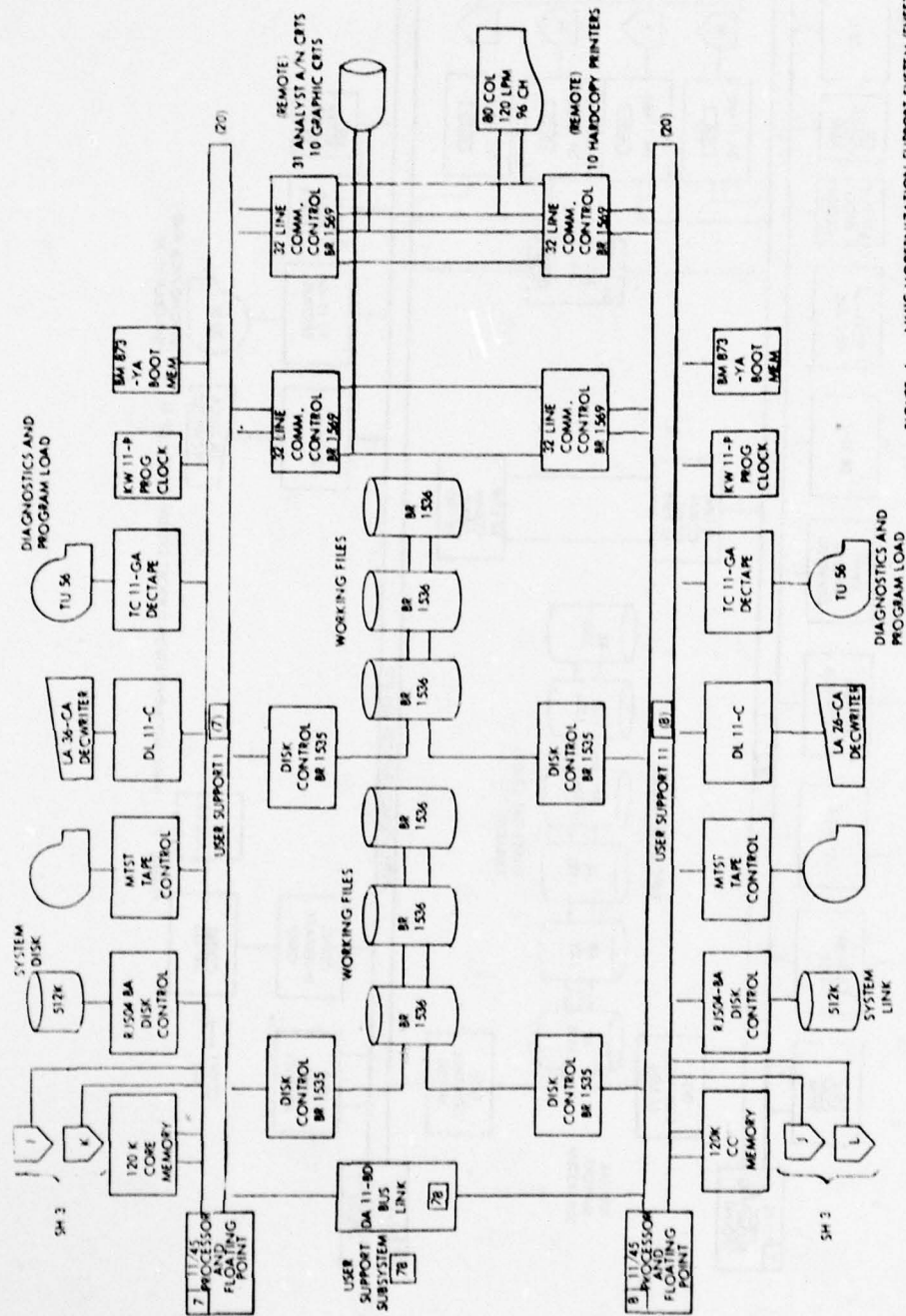
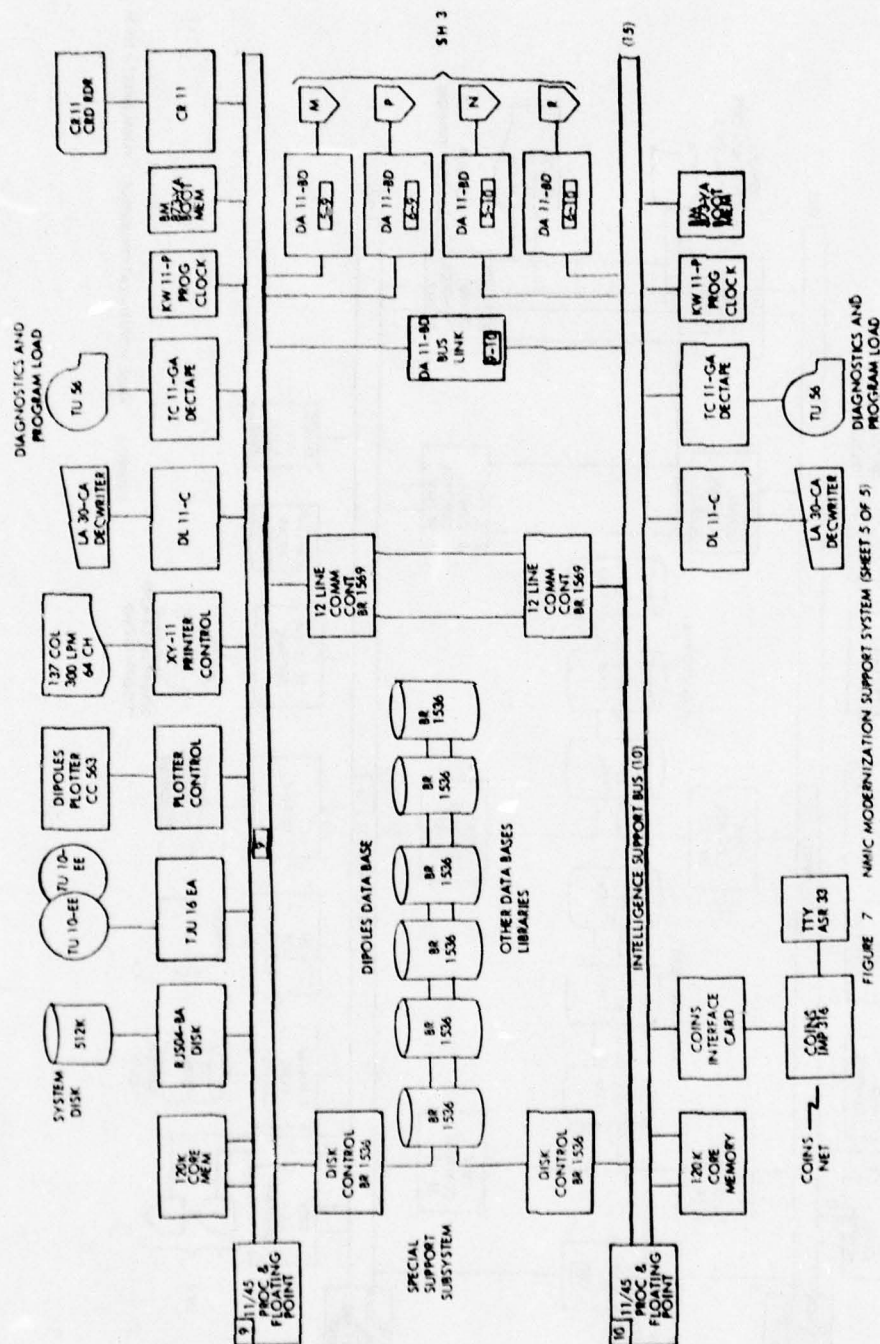
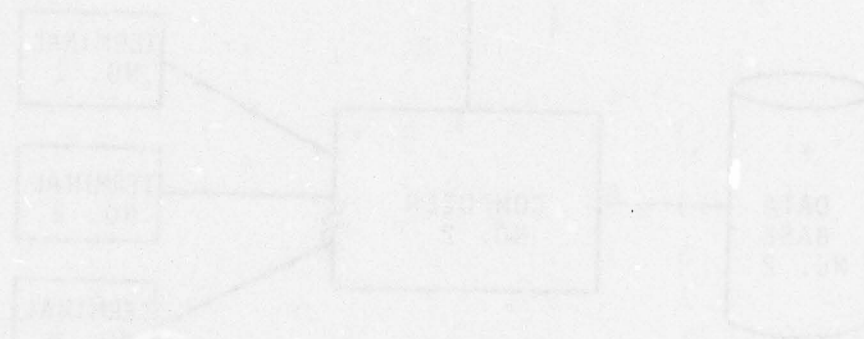


FIGURE 6 NMIC MODERNIZATION SUPPORT SYSTEM (SHEET 4 OF 5)



2.4 Typical Configuration of the IAS. There is no such thing as a "typical" AN/GYQ-21(V) configuration. NMIC is different from DIAOLS which is different from PACER, etc. There are perhaps no two applications that are identical. However, from a functional point of view, one configuration incorporates the essential features of the diverse applications. Figure 8 illustrates such a configuration. In general, there are more than one computer and data base involved. In the figure, two are shown. Each of the two computers has its own data base and set of remote terminals. A terminal user of Computer No. 2 can interrogate the files, that is, Data Base No. 2, as well as Data Base No. 1, via a telecommunications link, linking the two computers. In a similar way, a terminal user of Computer No. 1 can interrogate the files of both Computers 1 and 2.

The user control problem can now be stated. The user of a terminal is denied access to any records in either data base that without specific authorization, that is, security level, need-to-know, and intelligence compartment. The user is allowed free access to all other records.



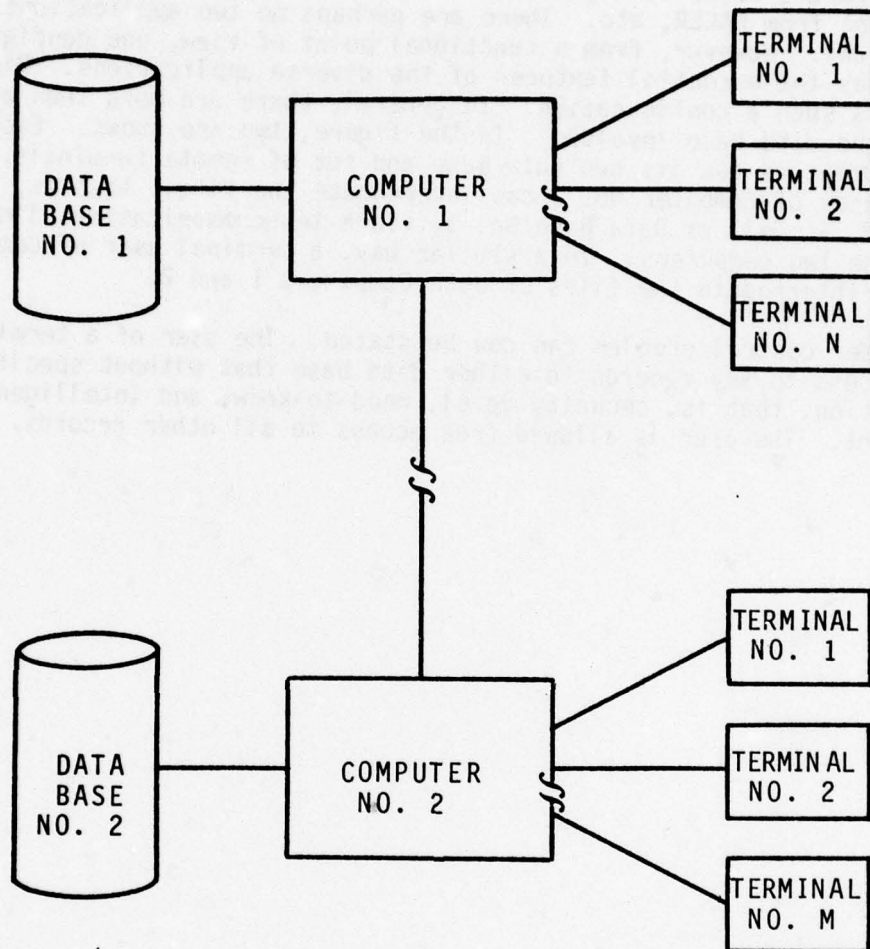


Figure 8 IAS ESSENTIAL FEATURES

THREAT

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3.0 THREAT

The primary measure of performance of a secure data base system is the ability to withstand a determined attack by a well-financed, highly-skilled enemy for a period of years, if not decades. To build such an impenetrable data base system requires a detailed knowledge of the tactics employed by a malicious user. What are the tactics that should be tried against candidate architectures? Fortunately, there are a number of books, papers and other communications on the subject. The "Computer Security Institute" periodically publishes reviews of books and papers on computer crime. A reader interested in a literature search on the subject is referred to Dr. Saltzer's article: "On-Going Research and Development on Information Protection."³ In this article on Page 23, Dr. Saltzer gives an index of abstracts on the subject and on Page 9, he identifies organizations having a capability in system penetration exercises. Among those listed in the article are Lawrence Livermore Laboratory, Information Sciences Institute, IBM Corporation Research Division, AF Electronics Systems Division and the Systems Development Corporation.

Unfortunately, the reports of criminal activity and the precise methods of the penetration teams tend not to get published. There is an understandable reluctance to publish criminal methods. There is one exception to this general rule and it is contained in a document that sets forth specifics on penetration tactics successfully used against MULTICS.⁴ That presentation is abstracted in part in this chapter.

Criminal attacks upon computer systems are pursued in two stages. First, the criminal gains command of the system by exploiting hardware flaws, software flaws or trapdoor. Next, the criminal proceeds to seize the protected data by use of any one of several tactics.

3.1 Criminal Tactics Given Command of the System. Suppose a User at a NMIC terminal somehow acquired the ability to read or write any word in PDP-11 memory. Subsequently, in this section it will be shown that it is quite easy to acquire such a capability. The criminal could then proceed with any or all of the following tactics:

- Dump the password file. Intelligence systems vary in the exact method used to log a user on the system initially. However, the procedure is generally as follows. The User requests the use of the system. The User is identified by name, social security number, and other identifiers. The system then requests a password which is a series of alphanumeric characters. If the

³Saltzer, Dr. Jerome H., Operating Systems Review, Vol. 8, No. 3, July 1974.

⁴Krager, P. A. and Schell, R. R. "Multics Security Evaluation: Vulnerability Analysis," AF Electronics Systems Div., ESD-TR-74-193, Vol. 2.

User provides the proper sequence, the computer assumes that the User is satisfactorily identified and is granted access. In the computer system is a file of passwords associated with each legitimate user. The malicious user can locate the start of the file in using the acquired ability to read data and read out the password file. With this capability the criminal can then masquerade as a user with higher privilege.

This tactic is frequently, though not always, countered by enciphering the password file. Still, if the code can be broken, the user can gain access to any information in the system.

- Falsify the access control list. Located beside the individual's identification is a list of access privileges. For example, one user might be permitted access to all Secret files while a user with higher privilege would be allowed access to all Secret plus all Top Secret files. The malicious user, by gaining access to the access control list, could change a privilege from Secret to Top Secret.
- Masquerading as a user with higher privilege. There is usually a word contained somewhere in the PDP-11 memory that identifies the current user of the system. Access privilege is checked against this individual. Using the capability to alter information anywhere in storage, the malicious user can change an identification to a user with higher access privilege.
- Falsifying logs. In the National Military Intelligence Center and other Intelligence Systems, all transactions are logged. The malicious user utilizing the capability to read and write memory, can falsify any logs and erase incriminating evidence.

There would be some difficulty in finding the critical words to read or write, but in practice this difficulty has not proved insurmountable. Listings are generally unclassified and are available. Even if this were not the case, locating critical words by trial and error can be accomplished in hours or days. Certainly not years or decades as prescribed by the performance criterion.

In addition to reading or writing, if the terminal user has somehow gained the ability to execute a set of instructions, beginning at some prescribed address, the criminal can also successfully execute the following tactics:

- Command the operating system to dump privileged data. The object of the attack is generally records stored on disk file. The disk file, in turn, is controlled by a device handler running under the operating system RSX-11D. By placing key words in the device handler and transferring control, the malicious user can proceed to dump any and all information in the data base.
- Write and execute programs that dump information in the data base. Even if the malicious user cannot locate the device handler, programs can still be written and executed to perform this task, thereby gaining access to all information contained in the data base.

The preceding list is by no means complete, but it will serve to illustrate tactics that can be effective for an espionage agent.

The criminal can also crash the system by writing into the operating system and by other means. Such sabotage attack is not in our view, considered serious, because service would be only denied a brief period of time. For example, in the National Military Intelligence Center, copies of the operating system are available on line and can be reloaded in a matter of minutes. Attempting to crash the system several times would place the criminal in a dangerous situation. For this reason, the study does not consider the problem of preventing a sabotage attack. Indeed, this is thought to be improbable.

The conclusion is obvious. If there is any way that the criminal can gain the power to read and write any one word of main memory, the time required for penetration of unauthorized data will be minutes or even seconds; rather than decades as prescribed by performance.

3.2 Gaining Command by Exploiting a Trapdoor. Trapdoors are unnoticed pieces of code which may be inserted into a system by a penetrator. The trapdoor would remain dormant within the software until triggered by the agent. Trapdoors inserted into the code implementing the reference monitor could bypass any and all security restrictions in the system. Trapdoors can potentially be inserted at any time during software development and use.

3.2.1 Example of a Trapdoor in MULTICS. Check\$Device-Name is a program that runs in Ring 0, the most privileged ring in MULTICS. Figure 9 shows an abbreviated listing of the code in PL-1 and the trapdoor.

The program is called with three parameters. The key which is the 72-bit binary string, Pointer 1 which points to a 36-bit word, and Pointer 2 which points to another 36-bit word. The trapdoor is inserted at the end of the program where it would normally return before exiting.

If key = bit____string____constant____password
is the coding that compares the 72-bit binary
word passed initially into the program with a
72-bit password.

If the two match, then the trapdoor program is executed. It appears on the following line.

then ptr2->overlay=ptr1->overlay.

The line of code simply says that the word to that ptr 2 points to is made equal to the word that ptr 1 points to. By swapping data between words pointed to, the trapdoor is able to read and write any word in memory, thereby allowing the malicious user to gain command of the system. Readers interested in details of the trapdoor are referred to Appendix C, Page 115 of the document referenced in Footnote 4 (Paragraph 3.).

```

check$device_name: procedure (a, b, code);

declare 1 code parameter,
        2 err_code fixed binary (35),
        2 key_bit (72) aligned,
        2 ptr1 pointer aligned,
        2 ptr2 pointer aligned;

declare overlay fixed binary (35) based;

/* Start of regular code */
...;

/* Here check$device_name would normally return */
    If key = bit_string_constant_password
        then ptr2 ->overlay = ptr1 ->overlay;

return;

end check$device_name;

```

Figure 9. Trapdoor in Check\$Device_Name

3.2.2 Data Base Query Trapdoor. The preceding example illustrated the basic principles of a trapdoor. There is a code which the user must know to trigger the door, but possessing this key allows the malicious user to gain command of the system. A limitation in the preceding example was that the word to be read out of memory is only transferred to another register and the word to be written is transferred from one memory location to another. In the NMIC, for example, as well as most other intelligence applications, the user does not have programming privileges, and, therefore, such a trapdoor would be of little use. However, this deficiency can be overcome quite easily by the data base query trapdoor.

Suppose there existed a trapdoor in NMIC that was triggered by some unlikely sequence of code typed by the user at a terminal, say QZKX. Suppose further that following the code the trapdoor would interpret the following instructions:

```

READ, (ADDRESS), causes the word to be typed on the terminal
WRITE, (ADDRESS) (NUMBER)
GO TO, (ADDRESS)
END.

```


With these commands the terminal user, even though being denied programming privileges, could fully command the PDP-11.

The trapdoor can be placed in the command interpreter software. However, in the case of NMIC, these are application programs, and the ability to read and write would be restricted to those prescribed by the application program. A powerful alternative would be to execute the trapdoor in the kernel state, and allow reading and writing in any part of the PDP-11.

3.2.3 Ease of Inserting and the Difficulty of Finding Trapdoors. Since the trapdoors are very small, sometimes only one or two instructions, they are difficult or impossible to detect in the large software systems used in the IAS. Frequently, such software runs in the tens of thousands of instructions and at times, it is in excess of a hundred thousand instructions. The trapdoor may be hidden in the object code. When this happens, the listings give no indication that the trapdoor exists. This tactic can be countered by recompiling at frequent intervals from source listings. Even so, the trapdoor may be hidden in the compiler and automatically reissued when the programs are assembled.

The threat of trapdoor insertion is further complicated by the ease with which a foreign agent would have access to the programs. RSX-11D is developed in an uncleared facility in Maynard, Mass. Although the application programs are developed by cleared personnel, the listings themselves are unclassified. The programs are communicated by open mail and sometimes by telecommunications. These provide further opportunities for the foreign agent to insert trapdoors. Finally, there is the possibility of a Trojan horse, i.e., a program being offered which is seemingly desirable, yet contains a trapdoor.

The threat of trapdoor insertion is most serious. If it is placed in the application programs, it will do little harm because the programs run in the user state and have restricted access to memory. However, if the trapdoor is inserted in the supervisory state, the malicious user would be able to command the device handler for the disk file, and be able to read and write any information contained in the data base. Finally, the trapdoor may be inserted in the kernel state giving the user complete command over the system.

The only known way of certifying that trapdoors do not exist is to prove the software does only what it is supposed to do. This task has proven impossible. In the case at hand, RXS-11D occupies some 26,000 lines of code. It is impossible to certify such a complex program.

3.3 Gaining Command of the System by Exploiting Hardware Flaws. It will now be shown, by example, that it is relatively simple for the computer criminal to gain command of the system by exploiting hardware flaws.

The experiment abstracted here is described in detail in the document referenced in Footnote 3, Pages 17 through 22. The MULTICS system on which the experiment was run has a virtual memory divided into segments with each segment broken down into pages and words. Access to memory for a given user is controlled by allowing access to certain segments and disallowing access to other segments. The descriptor segment contains the access privileges of that user. Such privileges include READ ONLY, READ AND EXECUTE, and NULL ACCESS.

In the reported experiment, a program was written to test the effectiveness of the access controls. The program was run under operating conditions in the background, once each minute for a period of 1100 hours and tested illegal instructions and access to restricted memory space.

As a result of the experiment, two errors were found in the hardware. The first was an undocumented instruction that did not appear to compromise security. The second was far more serious. It permitted the execution of instructions to bypass the access controls under certain prescribed conditions.

The execution of the "execute instruction access check bypass" proceeds as follows. There are three segments involved: the X segment in which the current user has READ and EXECUTE privileges, the Y segment in which the current user has READ ONLY privilege, and the Z segment in which the current user is disallowed access.

The program sequence is transferred to execute in Segment X. At a given location in this segment, an instruction is encountered that directs the execution of an instruction stored in Y 0. At Y 0 the instruction reads, "store the contents of the A register at location X 6." When location X 6 is read, there is an ITS command which directs the CPU to store the contents of the A register at location Z 0. Even though Z 0 is restricted to the user, the command is executed.

This vulnerability permits the user to read and write any word in a restricted memory location. As a result, the "execute instruction access check bypass" allows the user to initiate the tactics described in Section 3.1.

3.4 Exploiting Software Flaws. The reference in Footnote 4 sets as an objective finding one flaw each in hardware, software, and procedures. The software flaws were so plentiful that three were documented, Insufficient Argument Validation, Master Mode Transfer, and Unlocked Stack Base. These flaws are briefly described in the following paragraph. Readers interested in detailed information can reference Footnote 4, Section 3.3, Software Vulnerabilities, Page 22. These examples are chosen to illustrate how vulnerable a large hardware/software system is.

3.4.1 Insufficient Argument Validation. Suppose there existed a subroutine that executed in a privileged mode, in the example given, the mode was Ring 0 of MULTICS. For simplicity here, we assume it runs in the

kernel mode of the IAS. Since the subroutine runs in the kernel mode, it has access privileges to any part of memory.

The calling program runs in a much less privileged mode, Ring 4 in the MULTICS example. For purposes of illustration here, consider operating in the user mode in the IAS. Further suppose the subroutine can be made to store a word supplied by the calling routine at an address also supplied by the calling program.

Clearly, such a situation is dangerous because the calling program can make the subroutine write in any location of memory. For example, the calling program might choose to forge the user's identity by writing over the identity held in protected space. To prevent this from happening, on MULTICS every argument supplied by the calling routine is checked to see if the calling program has WRITE access privileges to the object address. This is termed Argument Validation.

Before discussing the vulnerability, it will be necessary to introduce two indirect modifiers used in MULTICS. The ITS modifier indirects the program by commanding DON'T STORE HERE, but rather in the location specified in the address field of this word. The IDC modifier (Increment Address, Decrement Tally, and Continue) redirects the location to that specified in the address field of the tally word after it has been incremented. Figure 10 taken from the document referenced in Footnote 4 illustrates the vulnerability. The argument supplied by the calling routine contains an IDC indirect modifier. The mistake in validation is to take the tally word address field before it is incremented rather than after. This leads to a first reference (shown at the right-hand side of the figure) which is checked by the validation routine. This seems to pose no severe problem because the address is just incremented by one from the second reference, which is the correct reference. However, if the two references are indirected a second time by an ITS modifier the object address can be in completely different parts of memory. Shown in the figure the second reference which is the correct reference directs to an argument which is writable only in Ring 0, while the first reference, the one checked by the validation routine, goes to an argument writable in the user ring.

Because of the insufficient argument validation, a user supposedly restricted to limited memory access can, in fact, write anywhere at all. Variation of this attempt would also permit the user to read any location in memory. With this capability, the malicious user could gain full command of the system.

3.4.2 Master Mode Transfer. In the MULTICS system, or rather the old MULTICS with ring-crossing software as implemented in the Honeywell 645, there existed a master mode procedure operating in Ring 4 called "Signaller." The function of Signaller was to communicate to the user certain types of faults. For example, if the user attempted to divide by zero, signaller would handle the fault by communicating the difficulty to the user. The result is that the Signaller program could be effectively

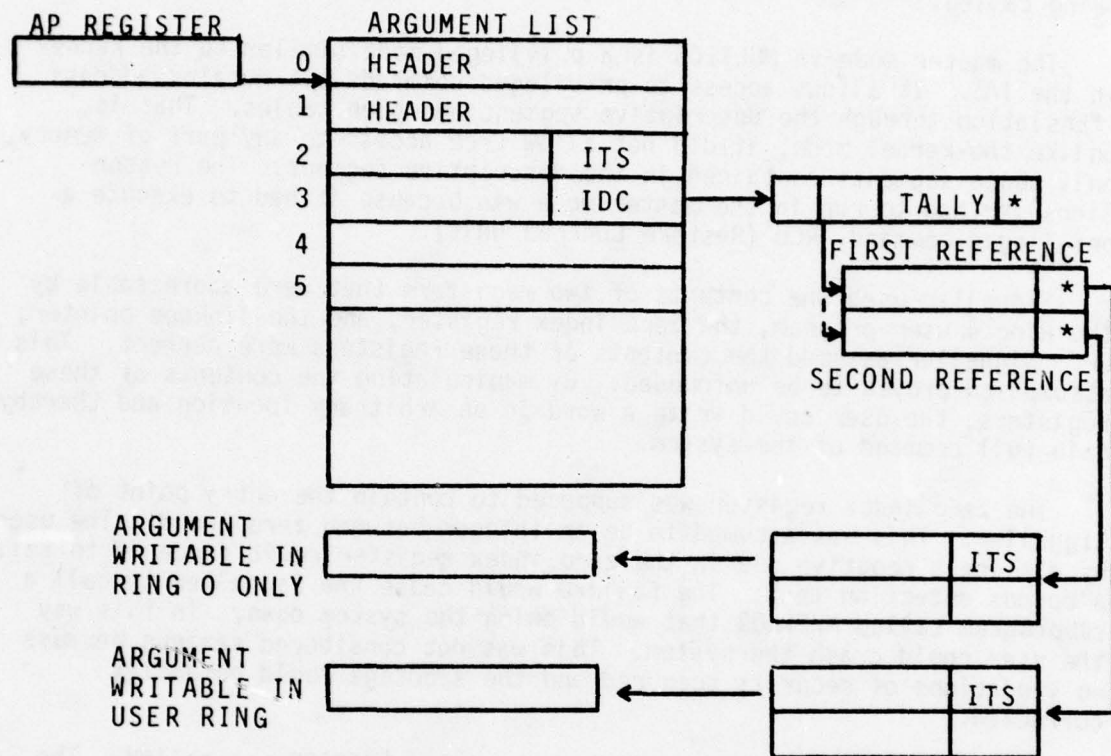


Figure 10 INSUFFICIENT ARGUMENT VALIDATION

called by the user program, also operating in Ring 4, by attempting division by zero or some other operation that would result in Signaller being called.

The master mode in MULTICS is a privileged mode similar to the kernel in the IAS. It allows access to privileged commands but retains address translation through the descriptive segment and page tables. That is, unlike the kernel mode, it did not allow free access to any part of memory, only those segments contained in the descriptive segment. The reason Signaller had to run in the master mode was because it had to execute a privileged command, RCU (Restore Control Unit).

Signaller used the contents of two registers that were addressable by the Ring 4 user program, the zero index register, and the linkage pointer, LP. Signaller assumed the contents of these registers were correct. This assumption proved to be unfounded. By manipulating the contents of these registers, the user could write a word in an arbitrary location and thereby gain full command of the system.

The zero index register was supposed to contain the entry point of Signaller. This was assumed to be an integer between zero and N. The user by placing a negative one in the zero index register could force it to fail a bounds detection test. The failure would cause the Signaller to call a subprogram called MXERROR that would bring the system down. In this way the user could crash the system. This was not considered serious because no violations of security occurred and the sabotage could be easily corrected.

The fatal software flaw occurred in the way MXERROR was called. The instruction was as follows:

```
tra lp|12,
```

that is, transfer to the address contained in the link pointer plus 12. Since the contents of the link pointer could be written by the user program, the user force Signaller to write a word in an arbitrary location still in the master mode. For example, the user can write the contents of the A register into a segment descriptor word that, in effect, would give the user program the ability to write into an arbitrary segment. In this way, a user can gain full command of the system.

3.4.3 Unlocked Stack Base. As seen in the preceding example, an important method of exploiting software flaws comes from the fact that the system registers, such as the link pointer (lp) are addressable by the user, yet privilege procedures assume, incorrectly, they point to prescribed locations. The unlocked stack base exploits a second register, the stack pointer. There are 8 pairs of registers in MULTICS each containing 18-bit pairs. Lp is the link pointer; lb is the linkage base; sp is the stack pointer, and sb the stack base. Originally, the stack base was locked, that is, it could not be changed except in master mode. Because

this proved to be inefficient, the stack base was unlocked, resulting in the ability of a user-mode program to change it arbitrary.

Figure 11 shows the listings for Signaller. It will be recalled that Signaller checks the contents of index register zero. When it finds a minus one in the register, it concludes the integer is out-of-bounds, saves the registers, and calls MXERROR, shown in the listing as tra lp|12, since lp|12 is assumed to point to MXERROR which will bring the system down. The second flaw occurs in the coding that stores the register. In particular, sreg sp|10 stores the index registers beginning at the location specified in sp|10. As a result of this, one register, specifically the AQ register, is transferred to the address contained in sp|14. If a user changes the sp register, the net result stores the contents of the AQ register at any location specified.

Figure 12 illustrates the operation of storing in an arbitrary location. The execution of the Signaller program results in storing the contents of the AQ register at location sp|14. The contents of the AQ register are set at exd bp|0; tra bp|2, that is, the command is execute double; the instruction whose address is contained in bp|0. Then tra to the instruction whose address is contained in bp|2. In the figure, it is shown that the trapdoor contained in sb|14 is placed in the emergency shutdown link. This is a segment which is seldom used by the system and it is convenient point to store the trapdoor.

Figure 13 shows how the trapdoor is used. The calling program is entered and sets up the base pointer register. Next, the calling program transfers control to Signaller. The lp register has been set so that when Signaller tries to call MXERROR, assumed to be at lp|12, it in fact calls the emergency shutdown link location where the trapdoor is held. The execute double instruction of the trapdoor directs to an instruction that commands the Q register to be loaded with the word from the calling stack frame. The second of the double instruction directs that the word stored in Q be stored at a prescribed location which happens to be in the calling frame. The prescribed location contains an indirect modifier which directs in the example the word be stored in the descriptive segment thereby forming a new segment descriptor word. The use of the trapdoor allows the calling program to write any arbitrary word anywhere in the system. The point at which the word is chosen to be written is a segment descriptor word which now gives the user privilege to access the prescribed segment. Again, this may be a segment that contains a user identification; therefore, giving the current user the right to modify his identity and again gain command of the system. The trapdoor allows the user to read and write an arbitrary word in the system, thereby gaining full command of the system.

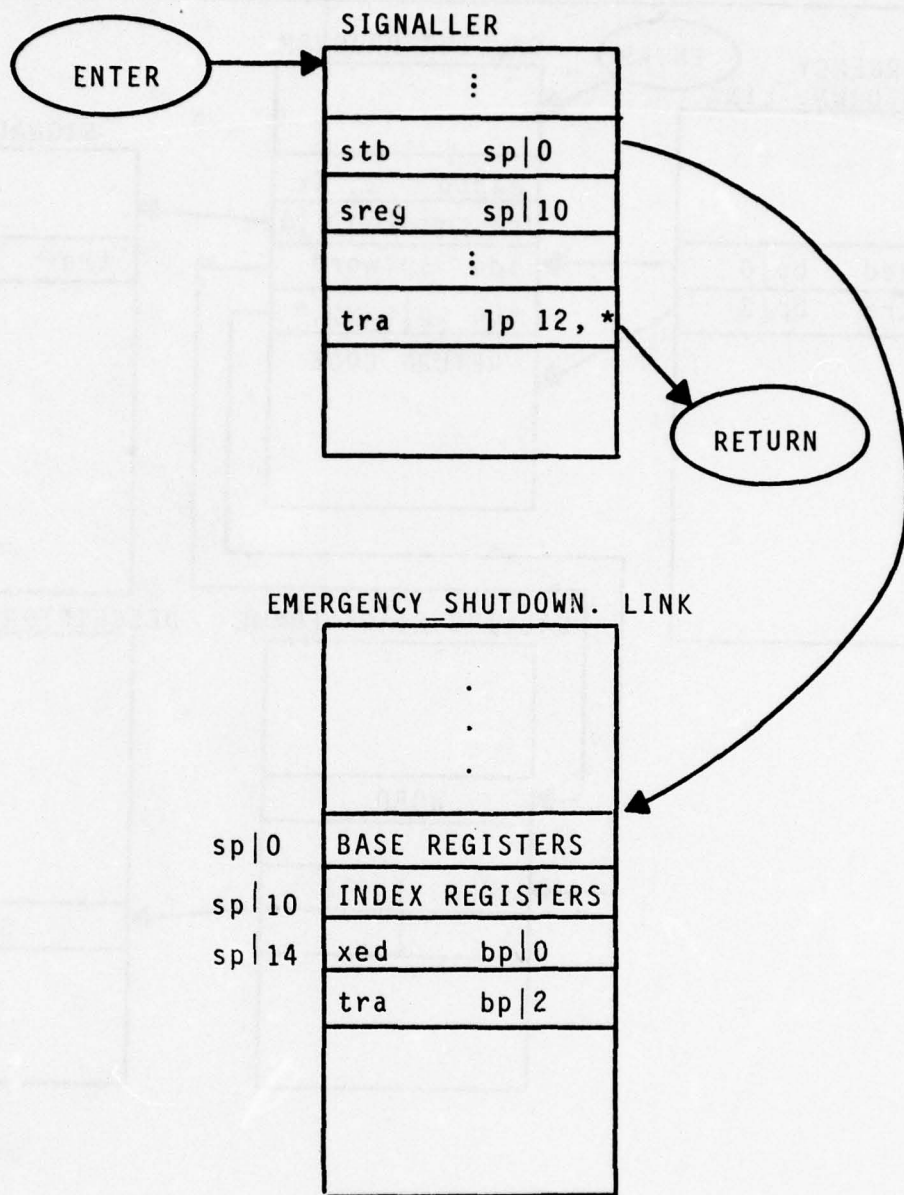
3.5 Penetration of RSX-11D. The major portion of this chapter is drawn from experiences reported by penetration teams. However, Harris did conduct its own penetration tests on RSX-11D during the course of the study. The test utilizing Method 1, described below, succeeded in


```

    cmpx0      2,du      "call in bounds?
    tnc        transfer_vector,0  "Yes, go to entry
    stb        sp|0      "Illegal call here
    sreg       sp|10     "save registers
    eapap      arglist   "set up call
    stcd       sp|24
    tra        lp|12,*    "lp|12 points to mxerror
a:  code
    ...
b:  code
    ...
transfer_vector:
    tra        a
    tra        b
    end

```

Figure 11. Master Mode Interpreted Object Code (Signaller)



AQ REGISTER :=xed bp|0; tra|bp 2
 INDEX 0 :=-1
 sp :=ADDRESS (UNUSED STORAGE IN EMERGENCY_SHUTDOWN.LINK)
 lp|12 :=ADDRESS (RETURN LOCATION)

Figure 12 UNLOCKED STACK BASE (STEP 1)

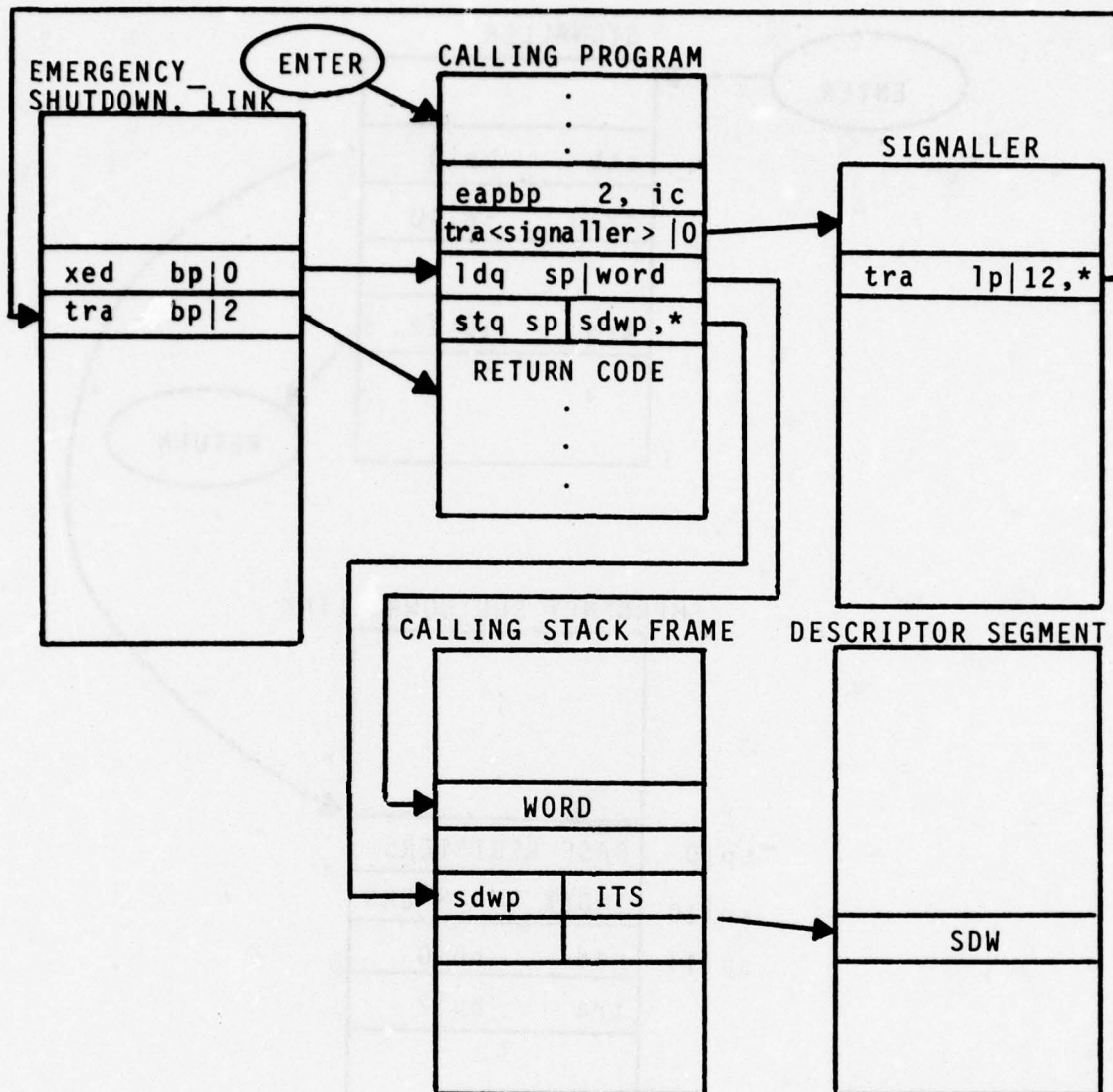


Figure 13 UNLOCKED STACK BASE (STEP 2)

approximately 2 hours. It is believed that if the attacker were properly trained, that RSX-11D can be penetrated in a few minutes.

The operating system RSX-11D for the PDP-11 series has the capability of providing password protection for a given user's data directory and/or individual files. The objective of the attack is to obtain the password of a file unknown to the user. Two methods of doing this are:

Method 1

- (a) Gain physical access to the machine control panel and an active teletype
- (b) Log in on user directory.
- (c) If user directory is password protected, enter a password but do not hit carriage return.
- (d) Halt machine.
- (e) Enter odd number into Register.
- (f) Press Continue.
- (g) Take core dump via dectape or magtape.
- (h) Run core dump analysis program.
- (i) Look for Task . . . HEL the login program.
- (j) Observe the needed password approximately 100 octal locations from the beginning of the task in standard ASCII encoding.

Method 2

- (a) Gain access to any terminal for the system.
- (b) Log in as any user number you know.
- (c) Run PIP (Peripheral Interchange Program).
- (d) Set default UIC to (11, 1).
- (e) Copy task . . . HEL into your user area.
- (f) Run ZAP program.
- (g) Make your copy of . . . HEL fixable in core by changing task header.
- (h) Run . . . HEL with Fixed in core option.

- (i) Type in user number of password protected user directory.
- (j) Use OPEN system directive to look into task . . . HEL at about 120 octal locations from the beginning of the task and observe the required password in standard ASCII.

3.6 Conclusions on the Threat. There has been no attempt in this chapter to exhaustively present criminal tactics. Rather, the intent is to give examples that have been effectively used in practice. These examples are intended to show the reasonableness of the ease with which a malicious user can penetrate the IAS.

Despite the limited number of examples shown, it must be concluded that there is no known way of preventing the malicious user from gaining command of the system. It has been shown that denying programming access will not work. The example of the data base query trapdoor illustrates that point. Further, there are undoubtedly combinations of hardware, software and procedural flaws that would achieve the same result.

We are forced to conclude that the malicious user can easily gain command of the system. The emphasis in the next chapter will be on examining the effectiveness of various architectural variations in view of this vulnerability.

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SECTION 4.0

EVALUATION OF CANDIDATE APPROACHES

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4.0 EVALUATION OF CANDIDATE APPROACHES

From the presentation in the preceding chapters, the problem of access control continues. Assume that the data base system shown in Figure 8 contains two types of variable length records stored on disk and has two types of users. The records are either Secret or Top Secret. Correspondingly, the user's privilege is either Secret or Top Secret. A user with Top Secret clearance can access any record in the data base, but the user with Secret clearance is denied access to Top Secret records. The problem is to prevent the malicious user with Secret privilege from getting Top Secret records.

The problem has been reduced to its essential elements. Obviously, if there were N compartments comprised of Unclassified, Secret, Top Secret, special intelligence access and "need-to-know" categories, the problem of restricting access would be similar, only more complex.

The problem of penetrating two or more computers is not really relevant. If the malicious user can gain access to a single computer in a matter of minutes, command of two or more computers can be accomplished in a brief period of time. While multiple configurations add some complexity, they do not change the essential problem.

The examination of alternative architectures is centered on the employment of external control mechanisms, as prescribed in the study's Statement of Work. The external control devices are sometimes referred to simply as "guards" or more commonly in the literature as "reference monitors." The guard terminology is more descriptive. The function of the reference monitor is analogous to that of a guard in a library containing secret and top secret information. The user provides identification to the guard and after the identification has been verified, the guard references the requestor's access list to find the user identification and privileges, that is, either Secret or Secret and Top Secret. The user requests a record and the guard checks to see that the classification of the record is authorized to that particular user, and either grants or denies access, depending on that determination.

The following paragraphs present a review of the deficiencies or vulnerabilities of the IAS as presented in the preceding chapter.

4.1 Existing IAS. As shown in the preceding chapter, the vulnerabilities of the AN/GYQ-21(V) fall into three categories:

- The criminal gains command of the system, that is, the ability to write anywhere in memory, dump single words or blocks, and execute arbitrary programs. This does not in itself accomplish espionage because the protected records of the intelligence system are stored in disk file, but it is a prerequisite first step.

- Given the ability to command the operating system or write programs that will dump the data base, the criminal proceeds to obtain a Top Secret record using a secret privilege.
- Alternatively, the criminal can attack the reference monitor or guard, that is, the mechanism in the IAS that guards access privilege to records, given the computer's understanding of identity of the requester and the access privileges.

Since gaining command of the system is a prerequisite to the other vulnerabilities, if modifications can be made to prevent this from happening, the IAS can be made impenetrable. What are these modifications? The first method is to eliminate the possibility of trapdoors or other flaws that can be exploited. Unfortunately, Harris does not know how to accomplish that objective. Testing for trapdoors and other flaws would be impossible.

The second method of preventing the criminal from gaining command of the system would be to build an effective reference monitor, that is, entrance guard that would prevent the malicious user from entering any unauthorized commands into the system.

4.2 Entrance Guards. An entrance guard is a reference monitor. It examines each request of the user and grants or denies the request, depending upon the privileges of that user. The reference monitor may be made impenetrable to attack by building it as an external device, totally isolated from the main computer system. The software in the reference monitor is small enough that it can be certified, thereby preventing it from being tampered with. Unfortunately, there is no known way to prevent the malicious user from bypassing the entrance reference monitor.

To see how a malicious user may bypass an entrance guard, it is first necessary to review the command language of the terminal. This varies from application to application, but Chapter 5 develops a language that may be used as an example, even though it is not typical. The commands are as follows: DISPLAY, PRINT, DELETE, ADD, and CHANGE. The ADD and CHANGE commands have the following structure:

ADD (report), NAME = nnnnn, DATA = ddddd.

The problem is the entrance guard has no way of telling whether or not the DATA hides a malicious command. Consider, for example, that the trapdoor could be triggered by entering QZKX, followed by a sequence of malicious commands outlined in the preceding section; READ, (address), WRITE, (address) (number), GO TO, (address), END.

Since the form of the trapdoor trigger and the commands are unknown to the reference monitor, it cannot detect them and, therefore, prevent them from being executed. It is conceivable that the user could be denied access to all commands except one; for example, the PRINT command,

reserving the data base modification commands to other terminals of higher privilege. Still, the malicious commands could be hidden in the PRINT format. It would be awkward, but far from impossible.

We are forced to conclude that entrance guards are useless as long as there is the possibility of trapdoors or other flaws inherent in the software. Therefore, we must assume the malicious user can gain full command of the system and explore methods of making the IAS impenetrable under this assumption.

4.3 Protected Access Controls. A necessary, but insufficient condition for an impenetrable IAS, (assuming the criminal can fully command the system) requires that the access control mechanism be protected from penetration attempts. Failure to protect the access control mechanism can result in falsification of user identification and access privileges. It is feasible to build an isolated, external access control mechanism that is secure from attempted tampering by a criminal.

The procedures for establishing user access privileges vary with different intelligence systems but generally follow this sequence:

- The user types in on the terminal a request for service. The sign-on includes user identification, charge number and other pertinent data.
- The computer commands the user to verify identification usually by requesting a password. The intelligence community has experimented with other means of identity verification including hand geometry, voice prints and fingerprints. However, an examination of the vulnerability of masquerading attempts is beyond the scope of the current contract. It will be assumed throughout, a simple password is adequate to verify claim identity.
- At this point in the sign-in dialogue, the computer is satisfied with the user identification and proceeds to consult the access list to determine user privileges, that is, either Top Secret or Secret.
- Finally, a computer system passes these access privileges to the reference monitor responsible for controlling access of that user.

In all intelligence centers, the sequence of sign-on control is physically contained within the IAS or large general purpose computer connected through the IAS. Obviously, if the criminal can command the IAS or the large computer system, (which must be assumed), then the user can freely change identity or access privileges.

Figure 14 shows a system to prevent this from occurring. The access control mechanism comprised of an access control center and a guard for each terminal is completely external to the IAS. In practice, the access control center would be a small minicomputer or a microprocessor. The

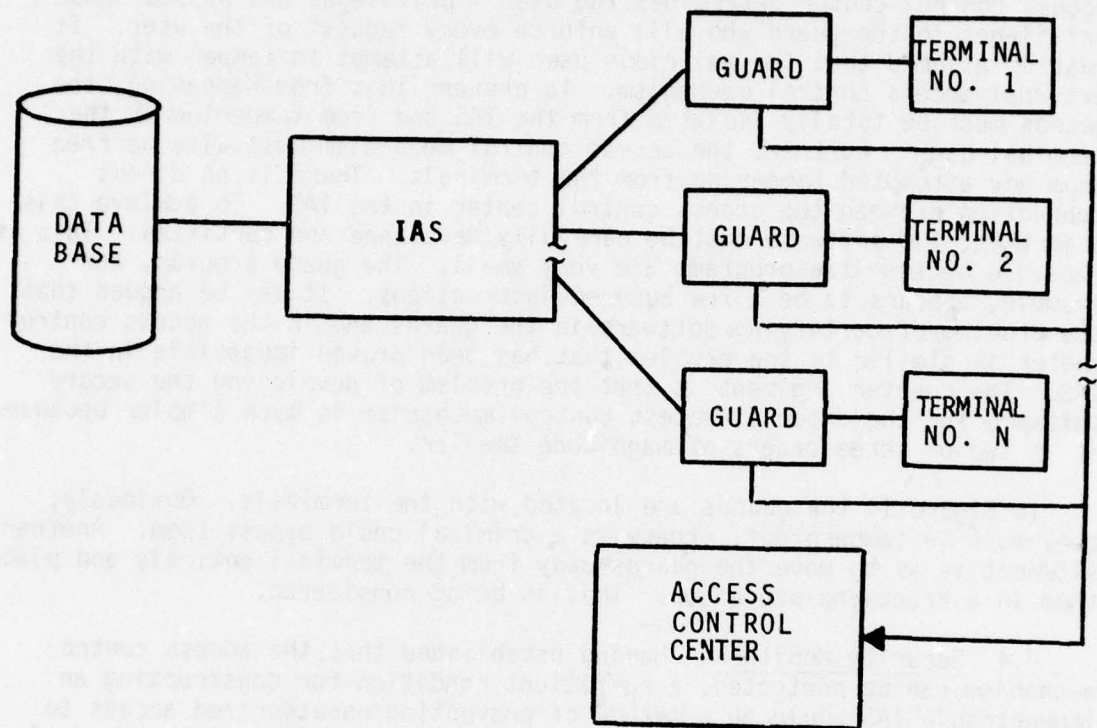


Figure 14 EXTERNAL, ISOLATED ACCESS CONTROL MECHANISM

guards would be microprocessors; in the feasibility model they are Digital Equipment Corp.'s LSI 11's. When the user signs on the terminal, the access control center determines the user's privileges and passes those privileges to the guard who will enforce every request of the user. It must be assumed that the malicious user will attempt to tamper with the external access control mechanism. To prevent this from happening, the guards must be totally isolated from the IAS and from tampering by the terminal user. Further, the access control mechanism must also be free from any attempted tampering from the terminals. There is no direct connection between the access control center in the IAS. To achieve this objective, the software must be carefully developed and certified. This is feasible because the programs are very small. The guard program, for example, appears to be a few hundred instructions. It may be argued that the problem of certifying software in the guards and in the access control center is similar to the problem that has been proven impossible in the IAS. The counter argument is that the problem of developing the secure software for the external access control mechanism is much simpler because it is two or three orders of magnitude smaller.

In Figure 14 the guards are located with the terminals. Obviously, they must be tamperproof, otherwise a criminal could bypass them. Another alternative is to move the guards away from the terminal entirely and place them in a front-end processor. This is being considered.

4.4 Security Monitors. Having established that the access control mechanism can be protected, a sufficient condition for constructing an impenetrable IAS would be a method of preventing unauthorized access to records, even though the criminal had command of the IAS. One method of accomplishing this is through the use of security monitors. Security monitors are an effective means to deter attempted espionage and are in use in the National Military Intelligence Center, the Defense Intelligence Agency On-Line System, and other intelligence systems. The theory of security monitors is to detect that a breach of security has occurred. This knowledge is often sufficient in itself, for it allows the criminal to be caught, keys to be changed, and generally to take measures to neutralize the negative effects of the espionage.

A problem with security monitors is the criminal can readily falsify the logs and erase the evidence. For specific examples of how this is accomplished, refer to the document referenced in Footnote 4, Paragraph 3.0.

4.5 Isolated Security Monitors. Just as it is possible to isolate and protect the access control mechanism, so it is feasible to isolate the security monitor, and prevent the malicious user from erasing the evidence. If erasure were the only problem associated with security monitors, that would be so. Unfortunately, it is not. They can be spoofed in the same way as the entrance guard. Suppose the user types in the sequence:

ADD (report), NAME = nnnnn, DATA = ddddd.

The data field may contain several hundred characters. Suppose the data field contains a trapdoor trigger and several commands to read and write privileged data in the IAS. The log believes the data item is a normal addition of a report to the file and has no way of detecting that it is, in fact, a malicious command sequence.

4.6 Data Base Guard. A method of denying user access to unauthorized records, even though the user commands the computer, has been proposed by Bob McGill of Harris. It is known as the Data Base Guard Approach.

Figure 15 illustrates the approach. The data base shown on the extreme left-hand side of the figure contains two types of variable length records, Secret and Top Secret. A multiported memory filters these records. IAS No. 1 is permitted all records in the data base, both Secret and Top Secret. IAS No. 2 is permitted Secret records only. IAS No. 2 may request a Top Secret record. The data base will be searched, but when the record comes to the multiported memory, the classification field will be sensed and the request aborted. The bottom of Figure 15 shows the organization of the record preceded by the classification field. The access control mechanism connects a user to one of the two processors, depending upon access privilege at sign-on. The engineering problems associated with this approach are threefold:

- Design and certification of the multiported memory - The multiported memory consists of a small microprocessor, hardware, and a brief program. An obvious penetration tactic would be to change the software or the hardware so as to allow Top Secret information to be communicated to the secret IAS. To prevent this from happening, design must be carefully executed and the software must be certified.
- Design of the access control mechanism - Obviously if a user with Secret privilege is switched to the Top Secret computer, all control is circumvented. The access controls would consist of an access control center which verifies the identity of the user and obtained user access privileges from a recorded list. It would then perform a switching function to the proper computer. This appears to be no serious problem and the design is not pursued further in this report since it appears to be straightforward.
- Cost - An IAS must be dedicated for each compartment. In the case illustrated in Figure 15 this is not a serious problem because there are only two compartments. In practice, however, there may be a dozen or more requiring that a large number of computers be purchased. The increase in cost is not as significant as might be expected. The central processing units are relatively inexpensive by comparison with the cost of peripheral equipment.

Harris believes the data base guard approach will prevent a malicious user from gaining unauthorized information. On the basis of this, we find that it is feasible to develop a secure data base system, although at

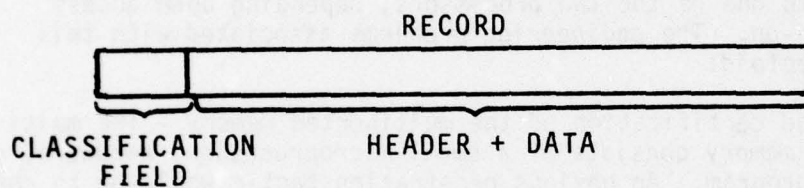
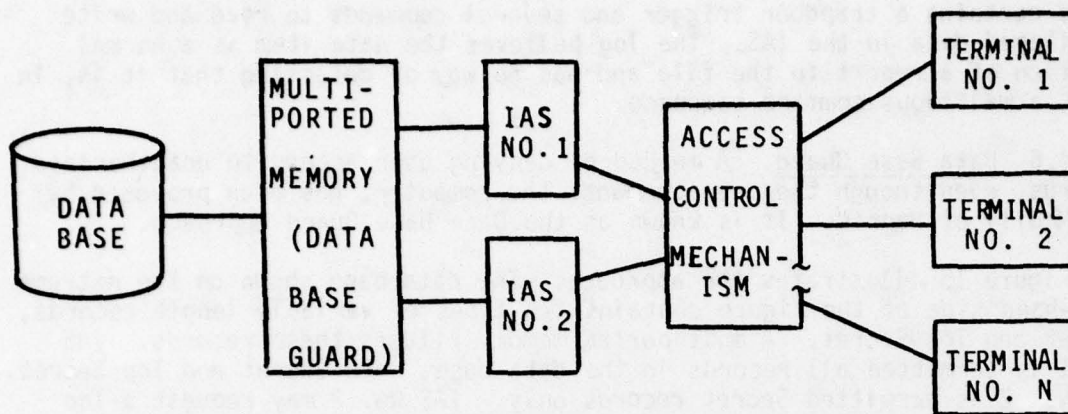


Figure 15 DATA BASE GUARD APPROACH

substantial additional cost. The search will continue for alternative approaches that are just as effective, but would incur less cost.

4.7 Tag Approach. A second method of securing records in the IAS has been proposed by Bob McGill of Harris. Suppose every record in the data base contained an 8-byte tag as shown in Figure 16 and the external access control mechanism operates as shown in Figure 14. The system operation would follow this sequence of events:

- The user begins the sign-on procedure and requests access to the data base system.
- Referring to Figure 14, the user input is recognized by the guard as the beginning of a sign-on procedure and control is passed to the access control center (ACC).
- The ACC accepts the request of the user which includes the user's Social Security number for identification and requests verification of the User's identity.
- The user types in the password.
- The ACC now accepts the user identified by Social Security number as a valid user.
- The ACC checks the access list colocated with the ACC. The list is comprised of Social Security numbers and the access privilege of each user (either Secret or Top Secret). Assume the current user has Secret privilege only.
- The ACC commands the guard to pass only Secret records to the user. Control is now passed to the user for communication via interactive dialogue with the data base system.
- The guard is totally transparent as the user queries the data base.
- A record is returned. The guard is able to discriminate between the various types of messages communicated from the IAS to the user and is able to recognize a record.
- The guard strips off the record tag to determine whether the record is Secret or Top Secret. If the record is Secret, the guard allows it to be displayed on the User Terminal. If the record is Top Secret, the guard does not communicate the record to the user but rather informs the access control center of a breach in security.
- After the classification has been established and before the record is communicated to the user, the guard checks for errors in the tag and errors in the message, utilizing the parity information as shown in Figure 16.

In evaluating the effectiveness of the tag approach it is first necessary to postulate the threat. Consider the threat of accidental disclosure. In that event, the 8-byte tag shown in Figure 16 is something of an overkill. All that is needed is a bit pattern to give the classification of the record and a field that identifies the record. It may also be desirable to include one or more parity bits to confirm that the security level is correct.

Considering the threat of malicious attack, the requirements on the tag approach are much more severe. First of all, if the tag is left in the clear, the criminal can be expected to falsify it, for example, changing the Top Secret classification to a Secret classification. Accordingly, the tag must be enciphered to prevent forgery. That is why the tag is chosen to be 8 bytes long; that is, the length of the block cipher used in the National Bureau of Standard Encryption Algorithm.

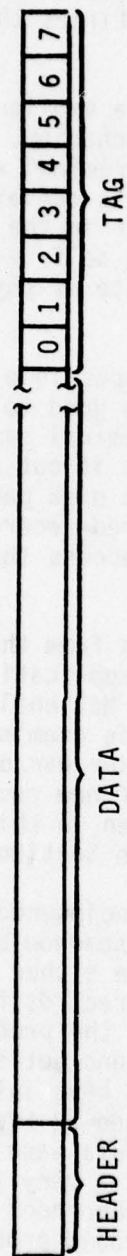
Even if a tag is scrambled, that in itself is not sufficient to prevent forgery. If the tag contains no parity bits or other record unique identifiers, the criminal can simply lift the tag from the Secret record and replace it on a Top Secret record. The purpose of the record parity bytes is twofold. It makes the tag unique and it provides a basis for determining whether or not the record is in error.

It is our opinion that the tag can be so designed as to be impossible to forge. Since the exit guard is so designed as to prevent the user from getting the requested record if the tag has been removed, mangled or otherwise fails to pass parity check, the user is denied unauthorized access; however, there remains the potential for bypassing the exit guard.

In a tag approach, it must be assumed the criminal commands a system and will try to get the record out past the guard any way possible. This situation is analogous to that of a burglar who has found the critical information, but there are exit guards posted at the exits that will inspect the document. Obviously, the burglar will try to get the information by the guard any way he can, by mailing it to himself, signalling out the window, throwing the information out the window placing it in trash collection barrels, etc. Figures 3 through 7 show the potential exits in NMIC. There are many tapes, disk packs, line printers and terminals which, if left unguarded, provide the potential for the malicious user to get the information out, including copying files and creating arbitrary messages. Accordingly, an effective exit guard system must guarantee there are no loopholes through which the malicious user can exit the information.

One way the malicious user would try to bypass the guard would be to disguise the classified information as an unclassified administrative message. One example is, if an operator types in an error, the system communicates back to the operator that error has been made. The error message could contain classified information. Unless the guard is able to distinguish between records and administrative traffic, the whole system will fail.

4.8 Enciphered Records. Suppose the data base were comprised of variable length records, each an integer number of 8-byte words (this is no problem in the IAS as the standard for disk retrieval is a sector length which is 256 words or 64, 8-byte words). A record requested by the terminal user is intercepted by the guard. There would be a clear text field identifying the record as such. The guard deciphers the record, reads the classification field, and matches the user's access privilege



TAG BYTES: 0 = RECORD CLASSIFICATION, TS OR S

1,2 = TAG PARITY, DETECTS ERROR IN TAG

3-7 = RECORD PARITY, DETECTS ERROR IN RECORD

Figure 16 RECORD TAG

against the classification of the record. If they match, the guard communicates the record to the user. If a Secret user has requested a Top Secret record, the guard destroys the record and notifies the access control center.

The initialization of the guard takes place in a similar manner to that of the tag approach, using an external, isolated mechanism. There are several schemes for passing the key. Obviously, the criminal will try to steal the key, and if successful, the whole system is defeated. One simple method of protecting the key is to manually place it in the guard and design the guard so that it is both tamperproof and self-destructs; that is, it is designed so that anyone trying to penetrate it physically erases the key from memory.

Because the records are enciphered and it is impossible to extract the clear text without the key, it does the criminal no good to bypass the guard. As in the case of the tag approach, the criminal can try to disguise the record as an administrative record, print it out on a remote printer, copy it on a disk pack, and then steal the disk pack, etc. For this reason, it is Harris' belief that the enciphered record approach is potentially a more effective means of controlling access than the tag approach.

The disadvantage of the enciphered record comes from the fact that the records cannot be processed. In all intelligence applications, some processing is required of the data base records. In the National Military Intelligence Center, for example, each incoming record is examined to determine to message addresses. Obviously, such an examination cannot take place on the enciphered record. This raises the question of how records can be processed when they are enciphered. The approach taken in this report is that of RED-BLACK multiprocessing described in detail in Section 6.0.

There are other problems associated with the enciphered record approach. First and most important is that all records must somehow be enciphered when they first enter the data base. This would require either an on-line device or a special batch processing step to prepare the records for the data base. This can add expense to the system. Then there is the problem of changing keys. If it is decided that the keys cannot be found out for a period of months or years, it is probably adequate to change keys infrequently, but if the Government determines the keys should be changed at frequent intervals, such as daily, this poses a severe problem. The data base would have to be read out and deciphered and reenciphered. This is a very slow process. Random access to a track in the IAS is in the neighborhood of 40 milliseconds. Reading and writing a record on the track could probably take place at speeds of not much greater than 20 records per second. Some of the intelligence data bases have several million records. Accordingly, the time to change keys could be very long.

4.9 Other Approaches. The architectural variations to the IAS to achieve information protection presented thus far are not exhaustive. There

are other approaches to prevent the unauthorized user from gaining access to records or removing records from within the IAS. Three additional approaches are briefly sketched below.

- Secure Software - If it were possible to develop software for the IAS that would be free of trapdoors and other flaws, then the malicious user would be denied the ability to command the system and thereby unable to gain unauthorized access. Consideration of a secure software approach is not within the scope of this study.
- Protected Index - A method that has been proposed to keep the malicious user from gaining unauthorized access to records is to hide the index. In the intelligence applications, the data base utilizes an inverted file structure. The theory goes that if the user cannot access the index, the record address is not available and access is denied. The weakness of this approach is twofold; first of all, the problem of preventing the malicious user from accessing the index, even if this can be achieved the user can still browse through the records and gain access to Top Secret records without authorization.
- Combinations of the Approaches - It may be possible to combine approaches such as the entrance guard and the tag approach, in order to achieve a high degree of protection. While the entrance guard is not foolproof, the tag approach has certain vulnerabilities. By combining them, one method may offset the weaknesses of the other. This approach of combining methods may have merit. It has not been pursued further in this report because other methods are viewed to be more promising.

4.10 Preliminary Findings. Of the ten approaches to achieving data base security in the IAS, seven were found insufficiently promising to merit further consideration. The remaining three ranked in order of their promise to provide the basis for an impenetrable IAS are as follows:

- Data Base Guard - It must be anticipated that a computer criminal would attempt to attack the access control mechanism that switches the user to the proper machine initially, and then attempt to attack the multiported controller that disallows Top Secret records from being read into Secret IAS. Of these vulnerabilities, switching mechanism seems to be a straightforward design and would offer little that the malicious user could attack. The multiported controller design is examined in detail in Section 7.
- Enciphered Record - The points of attack or potential vulnerabilities of this approach are the RED-BLACK multiprocessing, stealing of the key, tricking the exit guard into deciphering the data and cracking the code. Of these vulnerabilities, the RED-BLACK isolation is critical and is examined in Section 6. It is impossible to speculate on the other vulnerabilities without more detailed design information. Section 5 presents the design of a feasibility model to execute the enciphered record approach.
- Tag Approach - Potential vulnerabilities from this approach come from the potential for the malicious user to bypass the exit

guard by typing out the Top Secret record on other terminals, writing them on magnetic tape or disk pack and then stealing them or disguising them as administrative messages. The second potential for defeating the approach comes from forging the tag. The latter is not considered as serious as the former. Section 5 presents the feasibility model that can be utilized to design the tag approach and discusses the problem in more detail.

The latter two approaches assume the availability of a block encryption encipher/decipher device. The National Bureau of Standards 64-bit block encryption device may be utilized for non-Military applications. It is assumed that the Government will furnish a block encryption device suitable for Military applications. Because of this assumption, the potential of cracking codes to obtain enciphered records or falsify a tag are considered unlikely. For purposes of experimentation, a modified penetration evaluation requiring the use of a 128-bit key will be considered. Consideration will also be given to use of the Duffie Hellmen algorithm.

SECTION 5.0

AN EXPERIMENTAL, ENCIPHERED DATA BASE SYSTEM

5.0 AN EXPERIMENTAL, ENCIPHERED DATA BASE SYSTEM

The evaluation of candidate approaches presented in the preceding section established that three approaches have promise in building a secure data base system. Section 7 will present one of these approaches, the data base guard approach. It is considered less important than the other two because it is a brute force approach and requires the allocation of one computer central processing unit to each security compartment. This section discusses the other two approaches, the enciphered record, and the enciphered tag.

Since the initial objective of this study was to determine if the AN/GYQ-21V could be made secure for intelligence applications, the analysis of this section will establish that it is possible that either or both of the approaches will achieve the objective. In establishing feasibility, there are basically two approaches. The first is a theoretical analysis involving the design of critical characteristics versus cost. The other approach is to build the system or a portion thereof and see if it works. We believe that the experimental approach is superior in this instance to the analytical approach and, therefore, is used to examine feasibility.

5.1 Background. Before proceeding with the description of the feasibility model that incorporates elements of both the enciphered record and the enciphered tag approach, an overview will be given of this section.

5.1.1 Objectives. There are three objectives in developing the feasibility model:

- Develop a secure data base system. The primary objective is to establish that it is in fact possible by any method at all to prevent espionage in an intelligence data base system using the interactive analyst station.
- Quantify the relationship between the principal performance measure (time required to gain unauthorized access) and cost. It is not enough to prove academic feasibility but engineering feasibility must also be shown in this regard. The solution must be affordable and cost, or engineering design, becomes a prime consideration.
- Quantify the relationship between the other two performance measures (delay and reliability) and cost. The introduction of hardware for the external access control mechanisms will introduce delays in the processing of data base queries and other transactions. Further, the additional hardware introduced into the system will be a source of unreliability in operation. The extent to which performance is degraded will be explored as part of the study.

5.1.2 Method. Due to the limitations of funds, personnel and time, the analysis must be limited to those areas that will have the largest payoff. Primary emphasis will be placed upon the enciphered record approach. The problem of proving isolation between the red and black processors will be demonstrated in Section 7. The enciphered record approach has the engineering elegance of reducing access by encrypting the

entire record and is a method which has been demonstrated in telecommunications for decades to be an effective means of denying enemy access to information, even with free access to the encrypted data.

The first emphasis in the effort will go to the development of a feasibility model. Following this, at some later time (FY 78) the design and development of an engineering model will begin.

5.1.3 Message Flow in the Model. The model to be developed is representative of the types of data base systems encountered in the National Military Intelligence Center, and other intelligence applications. The flow of information can be visualized in five parts as follows:

- Operator enters transaction into the LSI-11 (guard). The operator requesting information or modifying the data base utilizes a terminal to communicate with the computing system. The terminal in turn is controlled by an exit guard in the case of the model simulated to be an LSI-11. The operator desires to execute certain transactions, such as QUERY THE DATA BASE, DELETE RECORDS, CHANGE or CREATE RECORDS. It is the function of the LSI-11, the exit guard, to control all of these transactions so as to achieve compartmentalized security.
- LSI-11 passes the transaction (query) to the 11/45. The exit guard has limited computing capacity and it is desirable that the software size be limited so that it may be certified. Accordingly, the processing is done in the main machine, in the case of the model being developed it is a PDP-11/45.
- PDP-11/45 returns all records that meet the search criteria to the LSI-11. The query requests all records that meet the search criteria, such as name, location, time, etc. The central processor searches the records and produces all those that meet the search criteria.
- The LSI-11 matches the record compartment against the user privilege. Two methods are implemented in the feasibility model, the tag method and the enciphered record. In the case of the tag method, the LSI-11 computes the parity on the enciphered record and compares parity with that contained in the tag. It further decipheres the compartment identification of the tag and matches that against the user access privileges. In the case of the enciphered record, the record is deciphered only if the user is authorized access to that record.
- If the user is privileged to that compartment, the records are printed. In either approach, if the user access privilege recorded in the guard matches that of the record that has been requested, the records are printed on the teletype printer.

5.1.4 Problems Examined by the Feasibility Model. There is a limitation of time and personnel available but it is desirable that the following performance measures of the feasibility model be examined and analyzed.

- Securing the number of responses to a data base query. In many intelligence applications, it is not enough to simply hide the records in the data base to prevent an unauthorized user from getting them, but it is also necessary to prevent an unauthorized user from finding out how many hits there are. For example, if a user was unauthorized to know the location of ships in a particular ocean, it might be possible for him to query the data base and find the number of ships in the Indian Ocean, thereby giving a certain amount of information.
The method of achieving denial of the number of hits to an unauthorized user in the feasibility model is to return all records that meet the search criteria to the guard, and upon request, print only the number of hits that the user has access privilege for; that is, the access rights of the user will be matched against each returned record and only those records that are authorized will be included in a tally of the number of hits.
- Transactions other than query. The primary emphasis in the feasibility model study will be upon query of the data base, based upon a number of keys and an "and" condition among those keys. There are, however, certain other transactions that must be studied. They are: DELETE RECORD, APPEND RECORD, CHANGE RECORD, CREATE RECORD. The method of handling these transactions is identical to the query transaction; that is, the user will be permitted to execute those transactions only if authorized.
- Administrative traffic. The operation of a terminal position requires that certain messages be exchanged with the computing system in addition to those of data base transactions. They might be, for example, communication of a message from one operator to another, messages on the status of the equipment, the number of records in a queue, etc. All messages must be controlled by the exit guard, otherwise the system may be defeated. For example, a malicious user could search the data base, get the information required, disguise it as an administrative message, and get it by the exit guard. To prevent this, all records must be tagged, administrative as well as data base operations.
- Enciphering algorithm performance. The most obvious way to defeat the security measures of the data base system is a direct assault upon the enciphering algorithm. The feasibility model will use a simple scramble algorithm which has little defense against a sophisticated agent. No attempt is made in the model to go to more sophisticated approaches. Although, as time permits, the National Bureau of Standards Encryption Algorithm will be explored as well as certain encryption algorithms based upon the principles of substitution and permutation sequence, and the Diffie Hellman algorithm. There is no attempt on the part of Harris to go into this problem area which is admittedly central to the overall performance of the data base scheme, but rather to obtain help from the Government. The design and development of enciphering algorithms is the sole province of the Government and it would not be wise to duplicate an extensive capability. Rather, we hope to obtain assistance on this matter.

- Sabotage prevention, detection and recovery. The design of the guard system is intended to detect deliberate efforts to falsify the tag or the record itself. This function is accomplished by the use of error detecting codes. When errors are detected, they are referred to the access control center, who examines the frequency of errors and initiates certain recovery procedures and alarms when they exceed an acceptable value.
- Espionage threat analysis. The design of the feasibility model is a vehicle for testing vulnerability. Certain threats will be postulated, including tampering with the guard, attempting to disable it, bypass it, or otherwise circumvent its operation. Additionally, certain privileged users, such as maintenance personnel, will be examined to determine whether the access controls can be defeated by somehow compromising these privileged users.

5.1.5 Summary. The remaining portion of the presentation of this chapter falls into five sections as follows:

<u>Paragraph Number</u>	<u>Title</u>
5.2	<u>LSI-11 (Guard) Top-Level Design</u>
5.3	<u>11/45 Top-Level Flow</u>
5.4	<u>Query Processing</u>
5.5	<u>Data Base Query Operations</u>
5.6	<u>Record Tagging and Detagging</u>

5.2 LSI-11 Top Level Flow. The experimental model should be as close as possible to the ultimate operational system. Accordingly, the central processor used in a PDP-11/45, which is software compatible with the AN/GYQ-21 (V). Preliminary sizing of the exit guard places it in the microprocessor category. For a first cut, the LSI-11 is used.

5.2.1 Exit Guard Design Approach. Figure 17 shows the equipment configuration used in the feasibility model. There are three principal parts. The exit guard and terminals, which control and initiate access, the access control center, and the central processing unit (11/45) used for storage and retrieval. Communication between the operators and the central processing unit, that is, the LSI-11's and the 11/45's, is via shared memory. There are three interactive analyst stations (IAS) simulated in the model. IAS No. 1 is an LA-36 local terminal used for entering and retrieving information in the central processing unit. IAS No.'s 2 and 3 have controlled access through the exit guard via the shared memory to the central processing unit.

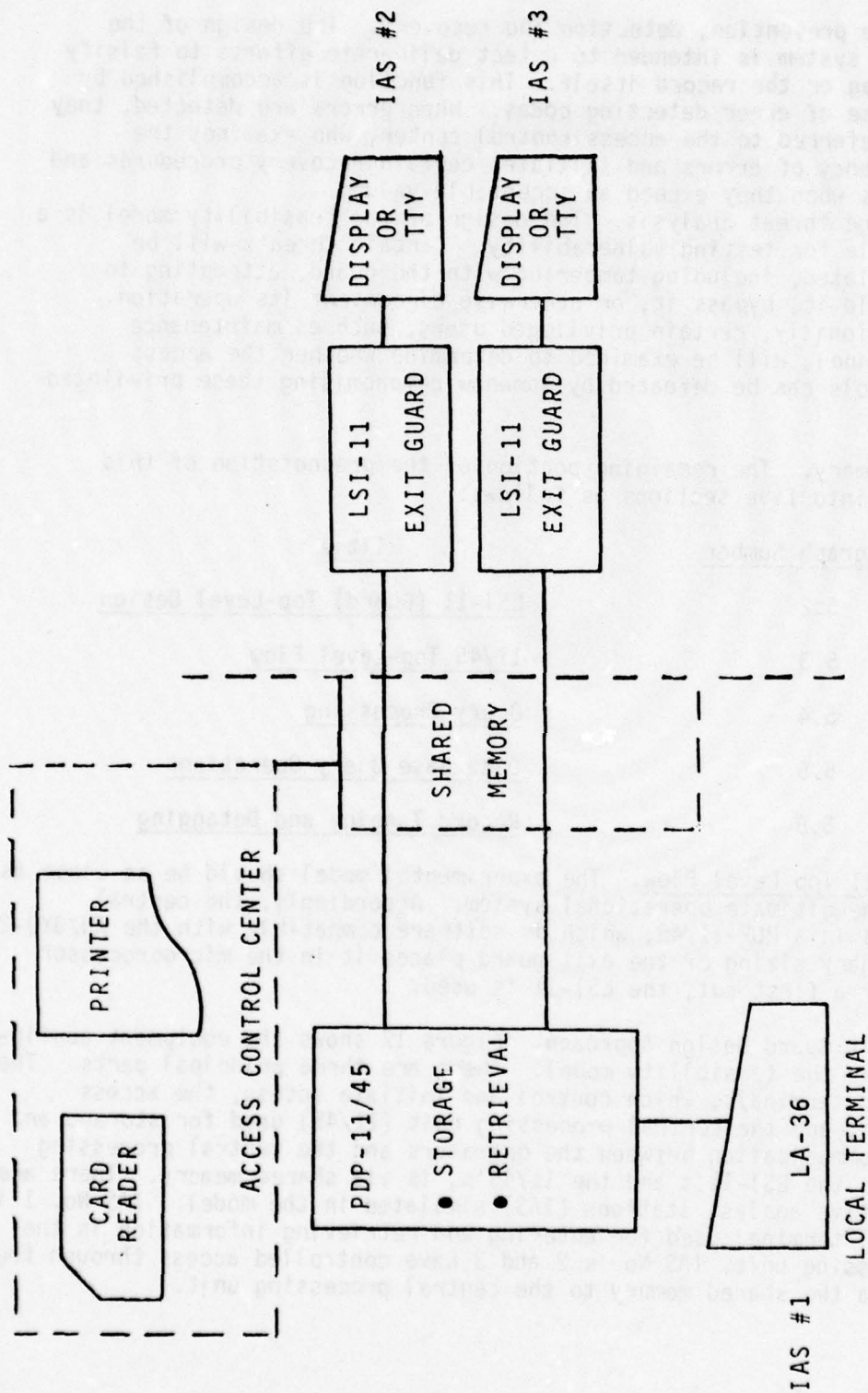


Figure 17
EXIT GUARD DESIGN APPROACH USING HESD'S COMPUTER ARCHITECTURE
DEVELOPMENT FACILITY

The access control center is, as the name implies, the central control for all of the exit guards. In the experimental configuration, it is comprised of a cardreader and printer. It passes the keys to the exit guards. The exit guards transfer control to the access control center when an anomaly occurs. In the operational system, the access control center will determine whether these anomalies are just accidental errors in the system or deliberate attempts on the part of a malicious user to penetrate the data base.

5.2.2 LSI-11 Top Level Flow. Figure 18 shows the overall program operation in the LSI-11. It is divided into two parts, initialization and operation.

The exit guard reads inputs from the keyboard. That is, it receives the characters and assembles them into messages. The carriage return is used by the operator to indicate a completed entry. Next, it processes the entry and communicates the results of the operator's input, that is, the assembled message, to the 11/45.

After the input message has been communicated to the 11/45, it awaits results. The results are in the form of a number of records which meet search criteria. When results are inputted from the 11/45, they are verified by the exit guard. This flow diagram utilizes the enciphered tag approach. Here the tag is verified; that is, the compartment contained in the tag is matched against the access privileges of the user. If the tag passes the test, the program branches to the good tag branch. If not, it branches to the bad tag branch.

If the tag is good, the record is communicated to the operator by printing or displaying it. If the tag is bad, a message is sent to the access control center and the records are not communicated to the operator. At the completion of each transaction, control is returned to the read keyboard module.

5.2.3 Initialization of the LSI-11. Table 3 shows the operation, purpose, inputs, and processing of the overall operation entitled, "Initialize the LSI-11." There are no outputs. The purpose of

Table 3. Initialize LSI

Operation:	Initialize LSI
Purpose:	To initialize the LSI-11 software and hardware prior to system operation
Inputs:	<ul style="list-style-type: none"> • Initial program load • Key for tagging and detagging record tags
Processing:	<ul style="list-style-type: none"> • Set up tables for tagging and detagging • Clear initial flags • Start keyboard inputs • Set up communications with 11/45 • Set up COMPOOL initial conditions

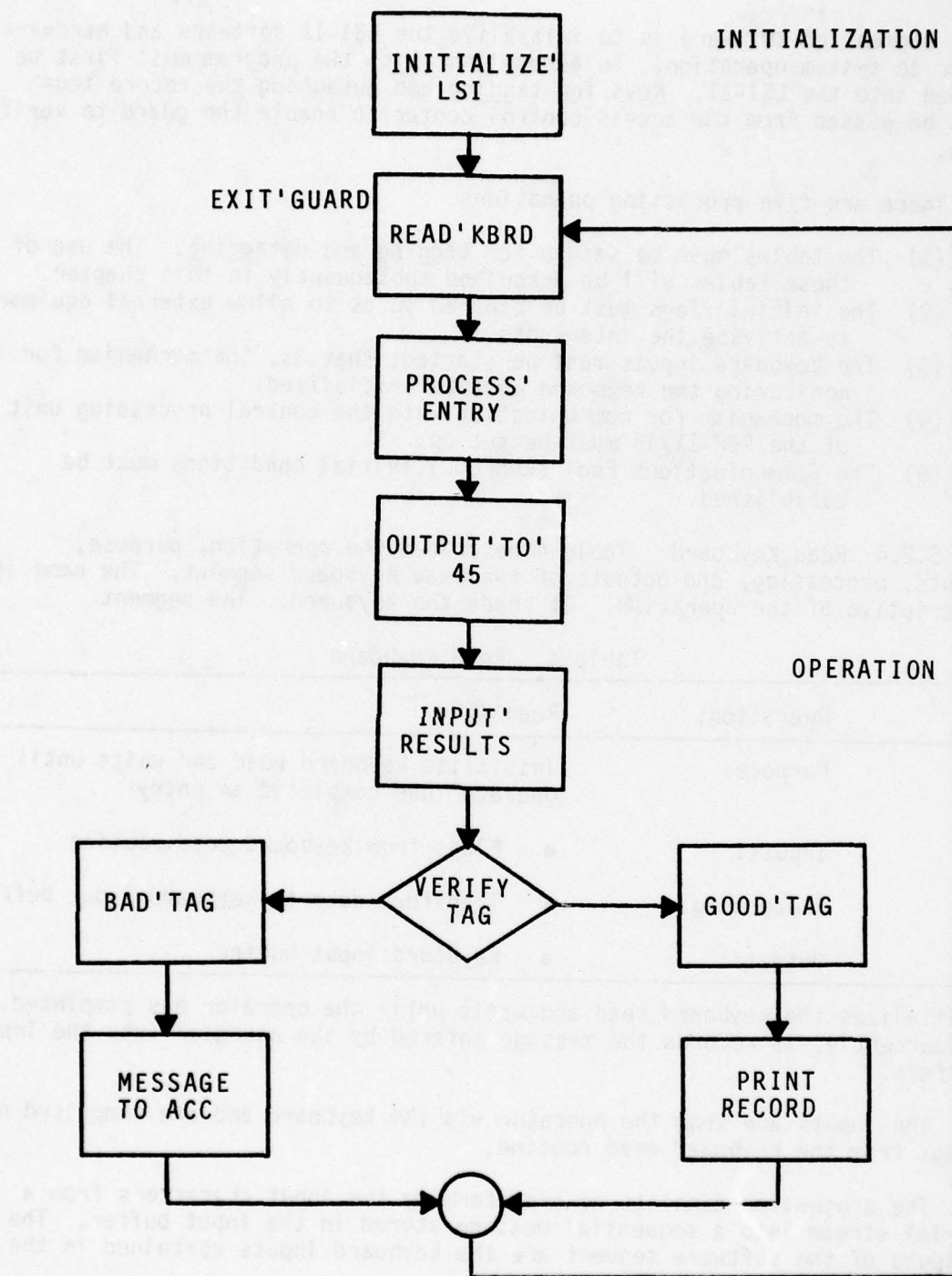


Figure 18 LSI-11 ISS TOP LEVEL FLOW

this segment of software is to initialize the LSI-11 software and hardware prior to system operation. To accomplish this, the program must first be loaded into the LSI-11. Keys for tagging and detagging the record tags must be passed from the access control center to enable the guard to verify tags.

There are five processing operations.

- (1) The tables must be set up for tagging and detagging. The use of these tables will be described subsequently in this chapter.
- (2) The initial flags must be cleared so as to allow external equipment to activate the interrupts.
- (3) The keyboard inputs must be started; that is, the mechanism for monitoring the keyboard must be initialized.
- (4) The mechanism for communication with the central processing unit of the PDP-11/45 must be set up.
- (5) The Communications Pool (COMPOOL) initial conditions must be established.

5.2.4 Read Keyboard. Table 4 described the operation, purpose, inputs, processing, and outputs of the Read Keyboard segment. The name is descriptive of the operation. It reads the keyboard. The segment

Table 4. Read Keyboard

Operation:	Read'KBRD
Purpose:	Initialize keyboard read and waits until operator has completed an entry
Inputs:	• Flags from keyboard read routine
Processing:	• Transfers data to keyboard input buffer
Outputs:	• Keyboard input buffer

initializes the keyboard read and waits until the operator has completed. Concurrently, it records the message entered by the operator into the input buffers.

The inputs are from the operator via the keyboard and are comprised of flags from the keyboard read routine.

The processing consists of transforming the input characters from a serial stream into a sequential message stored in the input buffer. The outputs of the software segment are the keyboard inputs contained in the input buffer.

5.2.5 Process Entry. Table 5 shows the operation, purpose, inputs, processing, and outputs of the process entry software. Before the message is assembled in its final form, certain processing takes place in the LSI-11. The purpose is to provide initial scanning of operator entry, to decode key words and provide error messages for improper messages. The process entry routine also accepts inputs or changes to the data base in the form of modifying, appending, changing, or entering a new record into the data base.

The inputs to the routine are the messages assembled in the keyboard entry buffer.

The processing consists of six steps.

- (1) The entry is scanned for key words.
- (2) The key words are replaced with mathematical operators.
- (3) The message from the keyboard is packed into a more dense form.
- (4) The program checks for an illegal entry, that is, an operator error in entering the command. If an error is detected, it is indicated to the operator and to the central processing unit, 11/45.
- (5) Control is returned to the exit guard.
- (6) The original operator inputs and changes made by the program are placed in a separate buffer.

Table 5. Process Entry

Operation:	Process Entry
Purpose:	Provide initial scanning of operator entry. Decode key words and provide error messages if not a proper entry. Accept inputs or changes to data base.
Inputs:	<ul style="list-style-type: none"> ● Keyboard entry buffer
Processing:	<ul style="list-style-type: none"> ● Scan entry for key words ● Replace key words with operators ● Pack keyboard entry ● Check for a legal entry as defined in 9340-77-74 ● If an error is detected indicate to the operator and 11/45. Then return control to exit'guard ● Channel inputs and changes into a separate buffer
Outputs:	<ul style="list-style-type: none"> ● Scanned keyboard entry buffer ● Error message to operator ● Error message to access control center

The output of the software is the processed message placed in the scan keyboard entry buffer. Detected messages are output to the operator. Error messages are also communicated to the access control center and monitored to determine if the operator is deliberately trying to deceive the system.

5.2.6 Output to the 11/45. Once the operator message has been accepted by the exit guard, it is passed by the guard to the central processing unit, the 11/45. Table 6 shows the operation, purpose, inputs, processing, and outputs of the software segment.

Table 6. 11/45 Output

Operation:	Output to '45
Purpose:	• Tag scanned keyboard entry buffer
Inputs:	• Scanned keyboard entry buffer • Key tables
Processing:	• Tag record • Request output to 11/45
Outputs:	Tagged record(s) to 11/45

The purpose of this program is to tag the scan keyboard entry buffer when such entries are comprised of new records to be entered into the data base. The initial tagging is necessary so that all records in the data base have a tag to enable retrieval. Once the records have been tagged, they are placed in a buffer for output to the 11/45.

The inputs to the program are the scanned keyboard entry buffer (output of the preceding program) and the key tables necessary to create tags for new record entries.

Processing is comprised of tagging records which will be described in detail subsequently, and a request for output to the 11/45. Outputs from the program include tag records to the 11/45.

5.2.7 Input Results. Table 7 shows the operation, purpose, inputs, processing, and outputs of the input results program.

Once the query has been communicated to the 11/45, the LSI-11 awaits input results. Inputs from the 11/45 are preceded by a signal. A transfer is initiated to the 11/45 input buffer of the messages which responded to the query.

The processing consists of waiting for the indication of results and the actual transfer of data from the 11/45. The outputs consist of messages contained in the 11/45 input buffer.

Table 7. Input Results

Operation:	Input Results
Purpose:	<ul style="list-style-type: none"> • Wait for results from 11/45
Inputs:	<ul style="list-style-type: none"> • Input signal from 11/45 • 11/45 input buffer
Processing:	<ul style="list-style-type: none"> • Wait for results indication • Transfer data from 11/45
Outputs:	11/45 input buffer

5.2.8 Verify Tag. Table 8 shows the operation, purpose, inputs, processing, and outputs from this program. It is assumed that the response to the input query resulted in a record being transferred from the 11/45. The purpose of the program is to operate the detag algorithm to establish whether or not the user will be granted access to the record which has been communicated.

Table 8. Verify Tag

Operation:	Verify Tag
Purpose:	<ul style="list-style-type: none"> • Operate detag algorithm
Inputs:	<ul style="list-style-type: none"> • 11/45 input buffer • Key tables
Processing:	<ul style="list-style-type: none"> • Perform detagging algorithm • If a good tag operate good'tag • If a bad tag operate bad'tag
Outputs:	<ul style="list-style-type: none"> • Results of detagging algorithm

The inputs are the record from the 11/45 and the key tables necessary in the detagging algorithm, to be described subsequently. The processing is the execution of the detag algorithm. If the tag is good, the program branches to the good tag branch. If it is bad, the program branches to the bad tag branch. The outputs consist of results of the detagging algorithm.

5.2.9 Good Tag. Table 9 shows the operation, purpose, inputs, processing, and outputs of the Good Tag Program. Its purpose is to output results to the operator. Results in this case are a record retrieved from the 11/45 in response to a query initiated by the operator. The inputs are the message communicated from the 11/45 to the input buffer and results of detagging.

Table 9. Good Tag

Operation:	Good'tag
Purpose:	Output results to operator
Inputs:	<ul style="list-style-type: none"> ● 11/45 input buffer ● Results of tagging
Processing:	<ul style="list-style-type: none"> ● Initiate output to operator ● Return control to exit'guard
Outputs:	<ul style="list-style-type: none"> ● Results of retrieval to operator

Processing consists of communicating the output records of the operator and returning control to the exit guard. The net result is the communication of those records retrieved to the requesting operator.

5.2.10 Bad Tag. Table 10 shows the operation, purpose, inputs, processing, and outputs of the Bad Tag Program. Its purpose is to block unauthorized data from being presented to the operator; that is, if the operator requested information from an unauthorized compartment the detagging algorithm would detect this and branch to the bad tag program.

Table 10. Bad Tag

Operation:	Bad'tag
Purpose:	<ul style="list-style-type: none"> ● Block unauthorized data from presented to the operator
Inputs:	<ul style="list-style-type: none"> ● 11/45 input buffer ● Detagging Results
Processing:	<ul style="list-style-type: none"> ● Return control to exit'guard
Outputs:	Output to access control center, ACC

The inputs are the message communicated from the 11/45 to the input buffer and the results of the detagging algorithm.

Processing consists of returning control to the exit guard without communicating the record to the operator. The output from this program is a message to the access control center (ACC).

5.3 PDP-11/45 Top Level Flow. Control to the data base system is through the PDP-11/45. Messages such as QUERY THE DATA BASE, DELETE RECORD, CHANGE RECORDS, etc., are communicated by the LSI-11 and executed in the 11/45.

5.3.1 Top Level 11/45 Flow. Figure 19 shows the flow diagram at the top level of the 11/45. The flow is divided into two segments: initialization and operation. Messages from the LSI-11 guard are processed by the input message lock. Next, the source of the message must be identified. There are five possible sources: Console 1, which is an LSI-11 No. 1; Console 2, which is an LSI-11 No. 2; Console 3, which is an LA-36 teleprinter; the card reader, or an unknown source. Once the message source has been identified, the actual program will run in the partition of that source so as to achieve multiprogramming.

5.3.2 Initialize 11/45. Table 11 shows the operation, purpose, inputs, processing, and outputs of the Initialize program. The purpose, as

Table 11. Initialize 11/45

Operation:	Initialize '45
Purpose:	<ul style="list-style-type: none"> ● Initialize 11/45 and LSI-11's ● Initialize all I/O drivers ● Use card reader to set up keys tagging ● Check disk protection codes
Inputs:	<ul style="list-style-type: none"> ● Initial conditions file ● Keys from card reader
Processing:	<ul style="list-style-type: none"> ● Set up I/O drivers ● Set up tagging I/O tagging keys ● Start access control center (ACC) module ● Start 11/45 and LSI systems
Outputs:	<ul style="list-style-type: none"> ● Key tables ● Initial conditions

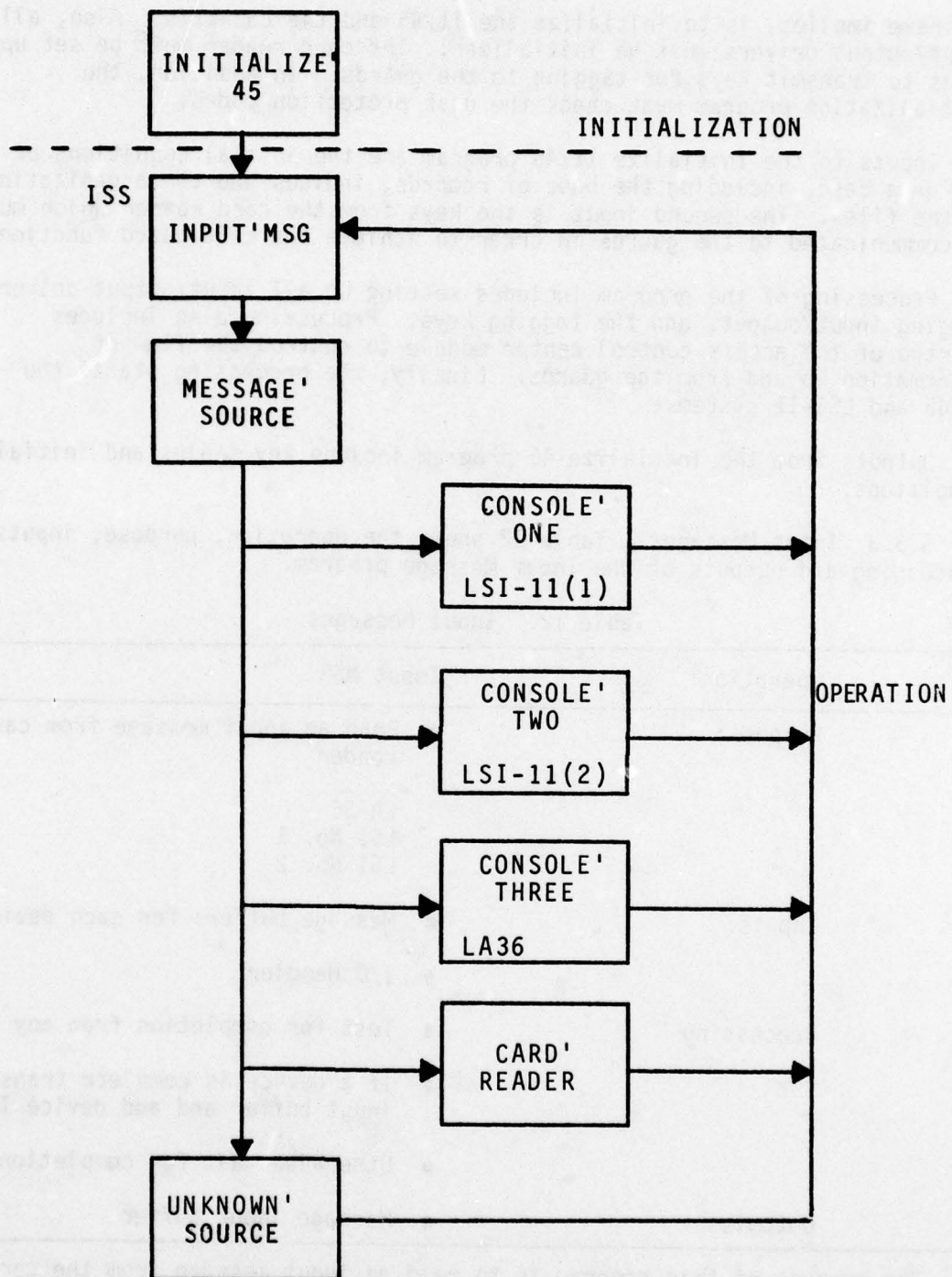


Figure 19 PDP-11/45 ISS TOP LEVEL FLOW

the name implies, is to initialize the 11/45 and the LSI-11's. Also, all input/output drivers must be initialized. The card reader must be set up so as to transmit keys for tagging to the guards. In addition, the initialization program must check the disk protection codes.

Inputs to the Initialize 11/45 program are the initial conditions of the data base, including the base of records, indices and the organization of the files. The second input is the keys from the card reader which must be communicated to the guards in order to achieve the exit guard function.

Processing of the program includes setting up all input/output drivers, tagging input/output, and the tagging keys. Processing also includes startup of the access control center module to control the flow of information to and from the guards. Finally, the processing starts the 11/45 and LSI-11 systems.

Outputs from the initialize 45 program include key tables and initial conditions.

5.3.3 Input Messages. Table 12 shows the operation, purpose, inputs, processing and outputs of the Input Message program.

Table 12. Input Messages

Operation:	Input MSG
Purpose:	<ul style="list-style-type: none"> ● Read an input message from card reader
	LA-36 LSI No. 1 LSI No. 2
Inputs:	<ul style="list-style-type: none"> ● Message buffers for each device ● I/O Handler
Processing	<ul style="list-style-type: none"> ● Test for completion from any ● If a device is complete transfer input buffer and add device ID ● Otherwise wait for completion
Outputs:	<ul style="list-style-type: none"> ● Message input buffer

The purpose of this program is to read an input message from the card reader, the LA-36, or either of the two LSI-11's. Inputs to the program include message buffers for each driver and an input/output handler.

Processing tests for the completion of any device. If a device is completed, the message is transferred to the input buffer and the device identification is added. If no devices are complete, the program waits for completion. Outputs from the program include messages in the input buffer.

5.3.4 Message Source. Table 13 shows the principal components of the message source program.

Table 13. Message Source

Operation:	Message' source
Purpose:	Test message source and transfer control to proper operation
Inputs:	<ul style="list-style-type: none"> ● Message input buffer
Processing:	<ul style="list-style-type: none"> ● Test message source and give to one of the following: <ul style="list-style-type: none"> - Console'one - Console'two - Console'three - Card'reader
Outputs:	<ul style="list-style-type: none"> ● None

The purpose of the software is to test the message source and transfer control to the proper operation; that is, the partition to be run on the multiprogramming.

Inputs to the program include messages residing in the input message buffer. Processing is comprised of testing message source and giving control to one of the following: Console No. 1, Console No. 2, Console No. 3, or Card reader. There are no outputs from this program.

5.3.5 Console One. The Console One program is intended to process all messages originating from that console. The purpose is to process Console No. 1's query; that is process in the sense of querying the data base or executing other commands originating at that console.

Processing is comprised of executing Console No. 1's query by tasking the query processing programs. The query processing programs are large and complex and are not covered in this section. After the query has been processed, control is returned to the main program. Outputs include the proper responses to the operator's query. Table 14 shows the major components of the Console One program.

Table 14. Console' One

Operation:	Console'one
Purpose:	Process console one's query
Inputs:	Console'one message buffer
Processing:	<ul style="list-style-type: none"> ● Process console one's query by tasking query'processing ● Return control to ISS
Outputs:	Query response

5.3.6 Console Two, Three, Card Reader. Table 15 highlights the functions of the other three programs that process sources of operator messages into the PDP-11/45.

Table 15. Console Two

Operation:	Console'two Console'three Card'reader
Purpose:	Process messages originating at consoles
Inputs	Console'two, console'three message buffer
Processing:	<ul style="list-style-type: none"> ● Process console two and console three's query by tasking query'processing ● Return control to ISS
Outputs:	Query response

The sources are the other consoles and the card reader. The inputs, processing, and outputs are identical to that of Console No. 1, except for servicing a different terminal.

5.3.7 Unknown Source. Table 16 shows the operation, purpose, inputs, processing, and outputs of the Unknown Source Program. This software is included to complete the processing of queries, even though identification of the message origin cannot be established. The reason for including this program is to provide an input to the access control center to detect attempts by malicious users to penetrate the data base system.

Table 16. Unknown Source

Operation:	Unknown Source
Purpose:	<ul style="list-style-type: none"> ● Process a message from an source
Inputs:	Message input buffer
Processing:	<ul style="list-style-type: none"> ● Count unknown messages ● If count exceeds a specific log that a penetration attempt been made ● Return control to ISS
Outputs:	<ul style="list-style-type: none"> ● Unknown message counts ● Penetration message

The inputs are from the message buffer. Processing consists of counting unknown messages. If the count exceeds a specific number, log a penetration attempt and return control to the central program. Outputs to the access control center include unknown message counts and penetration attempt warnings.

5.4 Query Processing. A major portion of software is devoted to the execution of data base transactions in the PDP-11/45. This processing is called query processing and is described in this section.

5.4.1 Top Level Flow. Figure 20 is a flow diagram of the overall query processing. The six blocks show the sequence of processing. Some of the processing is very complex and will be described in more detail in the appendix.

The processing operates on messages from one of the known sources. First the request is accepted, then it is passed to the generate intermediate language program. This is a reverse Polish notation scan that breaks the command up into a processing sequence.

If there are errors in the command, administrative error messages are sent back to the user, and the program exits. If there are no errors, the intermediate code is executed and the transaction results, such as updating or querying the data base. When processing results and messages to be communicated to the operator such as records matching the query key and conditions, the records are sent back to the user, and the program exits.

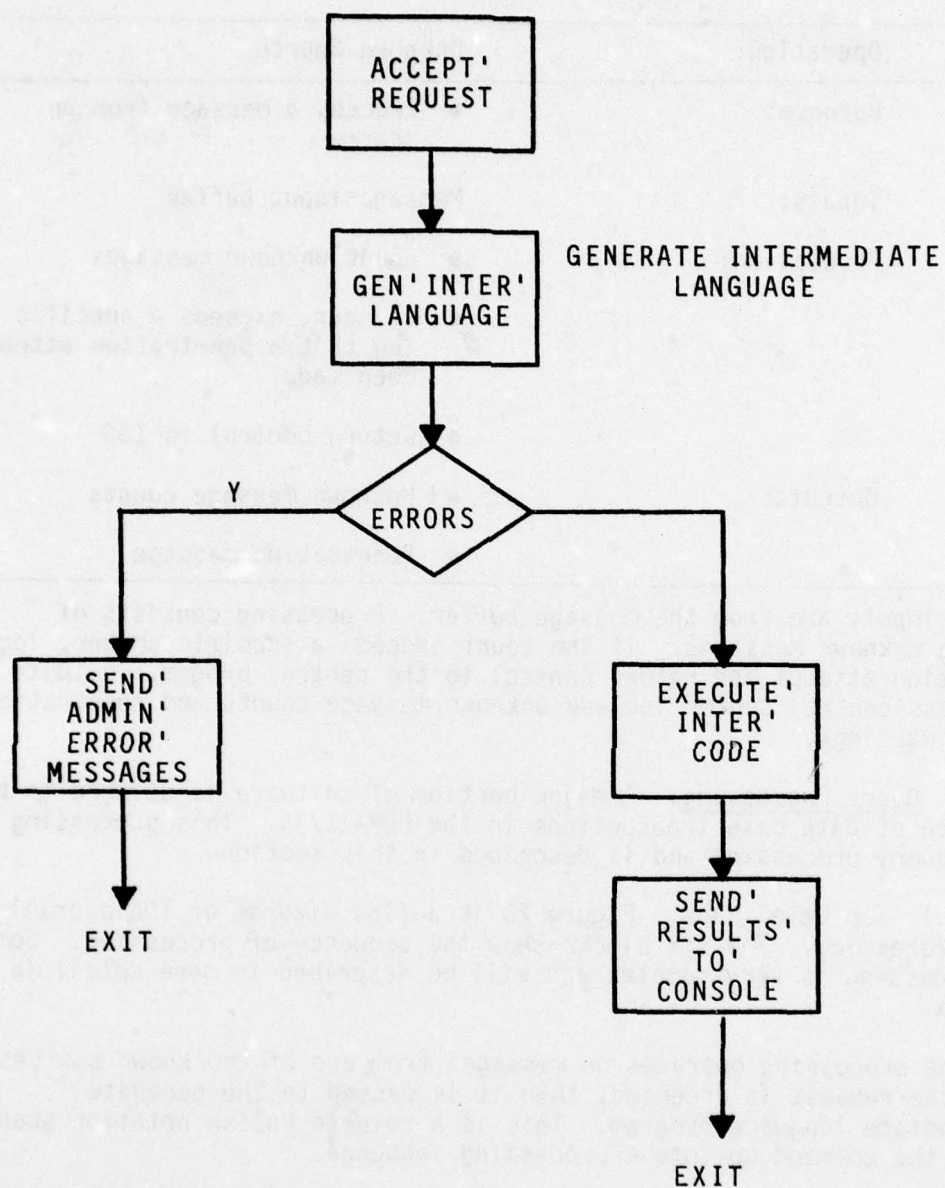


Figure 20 QUERY PROCESSING

5.4.2 Accept Request. Table 17 outlines the performance of the Accept Request program. Its purpose is to set up message buffer pointers for the generate intermediate language. Messages come in to the program via the message buffer, and the processing sets up pointers to the message buffer. Outputs are pointers for the generate intermediate language.

Table 17. Accept Request Number

Operation:	Accept'request
Purpose:	<ul style="list-style-type: none"> ● Set up message buffer pointers for gen'inter'language
Inputs:	<ul style="list-style-type: none"> ● Message buffer
Processing:	<ul style="list-style-type: none"> ● Set up pointers to message buffer
Outputs	<ul style="list-style-type: none"> ● Pointers for gen'inter'language

5.4.3 Generate Intermediate Language. Table 18 shows the operation, purpose, inputs, processing, and outputs of the Generate Intermediate Language program. The purpose is to scan query requests and generate intermediate code for execution by the intermediate language. Inputs to the program include message buffer pointers and communications pool data definitions.

Table 18. Generate Intermediate Language

Operation:	Gen'inter'language
Purpose:	<ul style="list-style-type: none"> ● Scan query request and generate intermediate code for execution by execute'inter'language
Inputs	<ul style="list-style-type: none"> ● Message buffer pointers ● Compool data definitions
Processing:	<ul style="list-style-type: none"> ● Perform a reverse Polish notation scan on the query and generate operational intermediate code ● If there are errors, do the following: <ul style="list-style-type: none"> - Count errors - Make a list of error numbers
Outputs:	<ul style="list-style-type: none"> ● Intermediate code ● Error count ● Error numbers

Processing on the command includes performing a reverse Polish notation scan of the query and generating an operational intermediate code. If there are errors in the command, the program counts the errors and makes a list of error numbers. Error messages will be communicated back to the originating operator. Outputs of the program include intermediate code, error count, and error numbers.

5.4.4 Errors. Table 19 shows the operation, purpose, inputs, processing, and outputs of the Errors program. Its purpose is to make a decision whether to operate the intermediate code. This is done only if there are no errors. Inputs to the program include intermediate code, error count, and error numbers from the preceding program. Processing proceeds if the error count is zero. In this case, control is given to the execute intermediate code program. If the error is greater than zero, control is passed to the program entitled, "Send Administrative Error Messages." There are no outputs from this program as it simply tests for errors.

Table 19. Errors

Operation:	Errors
Purpose:	<ul style="list-style-type: none"> • Make decision on whether to operate intermediate code
Inputs:	<ul style="list-style-type: none"> • Intermediate code • Error count • Error numbers
Processing:	<ul style="list-style-type: none"> • If error count is zero, give control to execute 'inter' code • If error count is greater than zero, give control to send 'admin' error messages
Outputs:	None

5.4.5 Send Administrative Error Messages. Table 20 shows the principal performance features of the Send Administrative Error Messages program. As the name implies, its purpose is to communicate errors back to the originator, when detected by the command interpreter. Input to the program includes error count, error numbers, message buffer, and error message file.

Processing consists of reading an appropriate message from the error message file and sending an error count to the console for each error detected. The program updates the error count for the console that

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originated the query. If the error count exceeds threshold, a warning message is sent to the access control center to provide an early indication of a malicious user operating at the terminal. Outputs from the program are error messages to the operator, error count for console, and access control center warning.

Table 20. Administrative Error Messages

Operation:	Send 'admin' error messages
Purpose:	Send operator error messages
Inputs:	<ul style="list-style-type: none"> ● Error Count ● Error numbers ● Message buffer ● Error message file
Processing:	<ul style="list-style-type: none"> ● For each error read appropriate message from error message file and send to console ● Update error count for console ● If error count exceeds threshold, send ACC warning
Outputs:	<p>Error messages to operator</p> <p>Error count for console</p> <p>ACC warning</p>

5.4.6 Execute Intermediate Code. Table 21 shows the operation, purpose, inputs, processing, and outputs of the Execute Intermediate Code program. The program is a large and complex interpretation of user messages into the data base. Its purpose is to execute the query request. Inputs to the program include intermediate language code.

Processing consists of executing intermediate code, storing the hit count, and the record number of the originating console in the hit table. Outputs from the program include hit count; that is, the number of records that meet the search criteria, and a hit table which lists the data base address next to each record.

5.4.7 Send Results to Console. Table 22 lists the major functions of the Send Results to Console Program. Inputs to the program include the hit count and hit table.

Table 21. Execute Intermediate Code

Operation:	Execute 'inter'code
Purpose:	Execute query request
Inputs:	Intermediate code
Processing:	<ul style="list-style-type: none"> ● Execute intermediate code ● Store record number in hit table for appropriate console ● Store hit count
Outputs:	<ul style="list-style-type: none"> ● Hit count ● Hit table

Table 22. Results to Console

Operation:	Send 'results to' console
Purpose:	Send results of query to console
Inputs:	Hit count Hit table
Processing:	<ul style="list-style-type: none"> ● If hit count greater than zero, send all records in hit table to console ● Otherwise send no response admin message to console ● Exit
Outputs:	<ul style="list-style-type: none"> ● Messages to console

Processing executes the command originated by the console operator. Specifically, if the hit count is greater than zero, send all records in the hit table to the console. Otherwise, send no administrative messages to the console. Outputs from the program include messages to the console in the form of records that meet the search criteria.

5.5 Data Base Query Operations. Thus far the flow diagrams have presupposed a language that the operator uses to interrogate and modify the data base. That language will now be described in this section.

5.5.1 Storage and Retrieval Block Diagram. Figure 21 shows the storage and retrieval block diagram. The data base is contained on disk file and is stimulated by query inputs. The queries result in a search to find the referenced records with the results of the query communicated to the operator. The data base may be updated either by the operators or by batch transactions.

In the enciphered tag approach, the record is broken up as it appears on the right-hand side of Figure 21. The first word of the record message packet contains the length of the record. The second word of the record contains the length of the data. The third word contains a description of the data; that is, whether it is an event or report. This is followed by the information itself and is used by the data base guard to control access.

5.5.2 Terminal Input/Output Block Diagram. The terminal illustrated in Figure 22 is the means of communication between the operator and the feasibility model. The operator inputs messages, and the terminal outputs the messages, either by printing or displaying them. The terminal includes the data base guard, which is responsible for the data tagging and detagging algorithms. The keyboard is the means of man/machine communication and the display presents the output results.

5.5.3 List of Statements. The language by which the operator communicates with the data base system allows a great deal of flexibility and is a powerful tool for querying and updating the data base. There are five statements:

- Display
- Print
- Delete
- Add
- Change

5.5.4 The Display Statement. The Display statement allows the operator to query the data base and select records which match the correlation criteria. Display has the following format:

Display	All		If Condition
	Type		
where:	Find	=	Find statement
	Type	=	Specific record type (such as report)
	All	=	All records which qualify
	If	=	If statement
	Condition	=	If statement condition

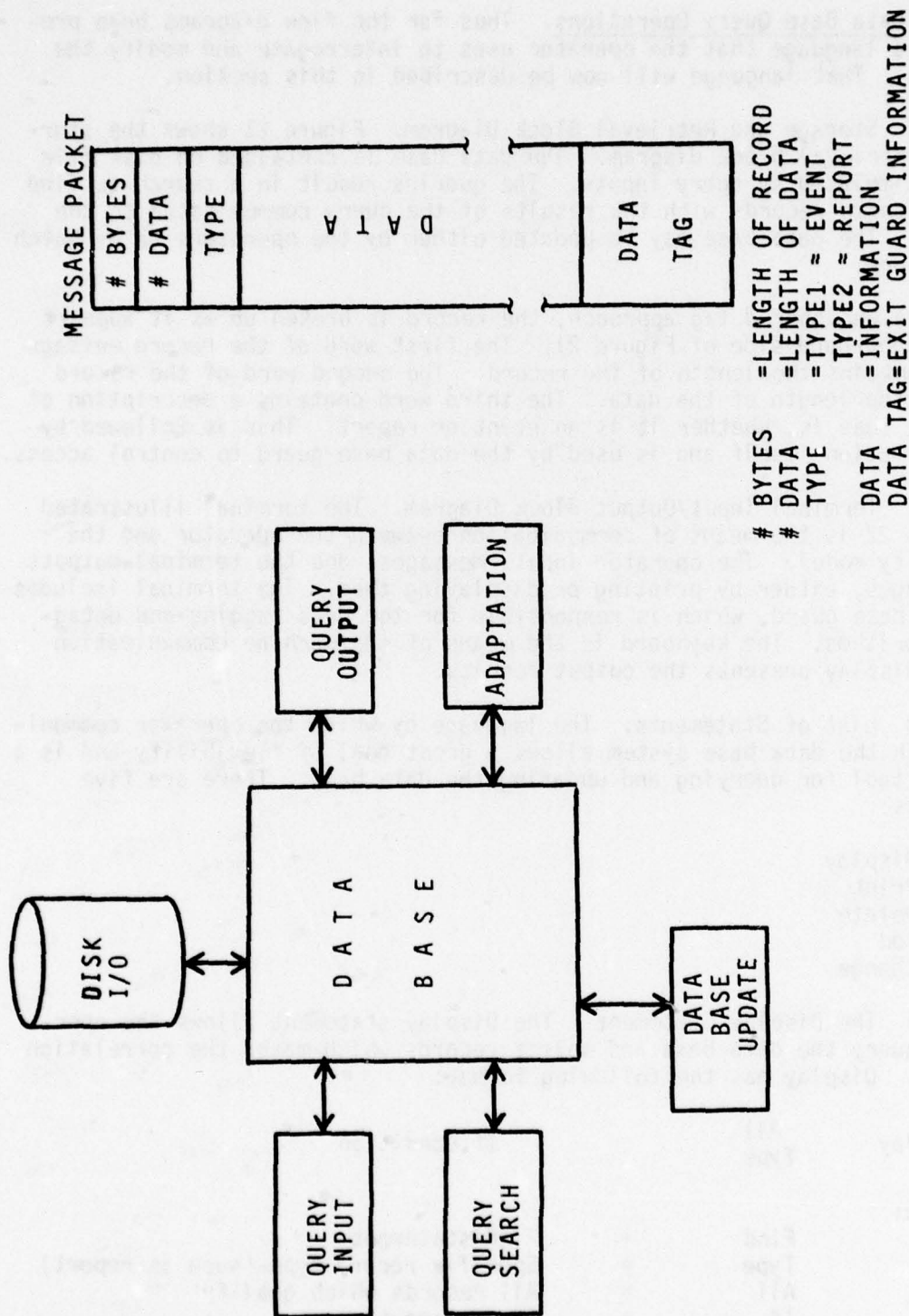


Figure 21 STORAGE AND RETRIEVAL BLOCK DIAGRAM

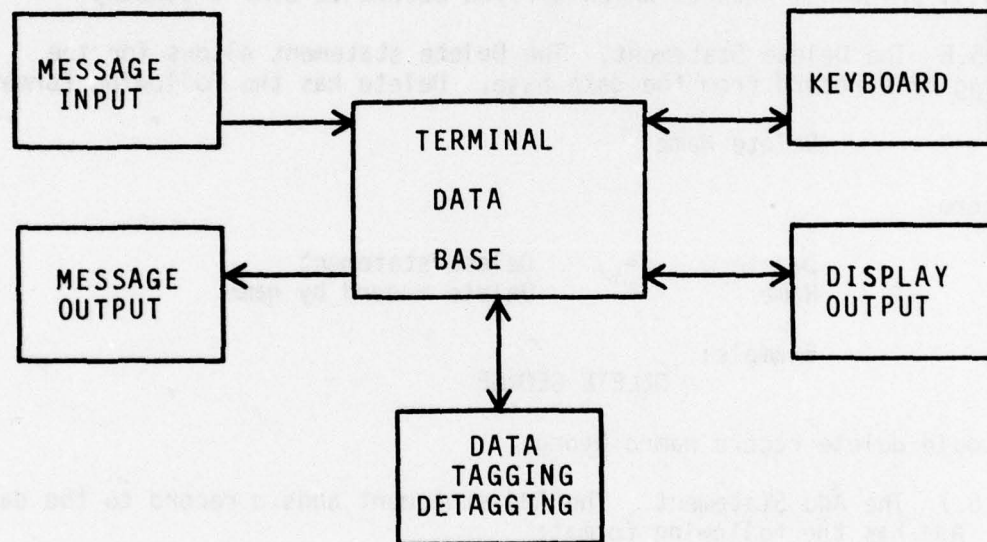


Figure 22 TERMINAL I/O BLOCK DIAGRAM

Example:

DISPLAY REPORT IF NAME EQ GEORGE

This will search the data base for a report with the name of George and display it if found.

5.5.5 The Print Statement. The Print statement allows the operator to print instead of display a record. Print has the same format as the display statement, except print replaces display.

Example:

PRINT ALL IF TIME LS 1 1200

This will print all records which arrived before 12 a.m. 1 January.

5.5.6 The Delete Statement. The Delete statement allows for the deleting of a record from the data base. Delete has the following format:

Delete Name

where

Delete	=	Delete statement
Name	=	Delete record by name

Example:

DELETE GEORGE

This would delete record named George.

5.5.7 The Add Statement. The Add statement adds a record to the data base. Add has the following format:

Add	Report	Name	=	nnnnn	data	=
	Event					

where

Add	=	Add statement
Report	=	Report type record
Event	=	Event type record
Name	=	Name identifier
nnnnn	=	Name of record (up to 30 characters)
Data	=	Data identifier

If report alphanumeric characters
If event then parameters on Compool
names of items in an event record.

Example:

ADD REPORT NAME = GEORGE DATA = This is a
report about George. Date 1 January 1977.

This would add a report to the data base with the name "George" and the data as indicated above.

5.5.8 The Change Statement. The Change statement allows the operator to change a record. The Change statement has the following format:

Change Report
 Event Name = nnnnn Data =

where:

Change = Change statement
Report = Change report
Event = Change event
Name = Name identifier
nnnnn = Name of record to be changed
Data = Data deletemeter followed by Compool items or
 report text to be changed.

5.5.9. The If Statement. The If statement is used in conjunction with the display or print statement. If is the search argument of the Display and Print these statements. The format of If is:

If Condition

where:

If = If statement
Condition = Logical condition i.e., where:
 CC = logical operator
 EQ = equal
 LS = less
 GR = greater
 LQ = less or equal
 GP = greater or equal
 CN = connectors
 or
 and
 A, B, C, D ... N = are expressions

Example:

IF TIME GR 2140Z AND RANGE LS DISTANCE - 256
Condition is true if time is after 2140Z and
range is less than distance -256 miles

5.6 Simplified Record Tagging and Detagging. Although the emphasis in this section is to describe one of the two methods, namely, the enciphered

tag approach, the other approach, enciphered record, will also be explored in the feasibility model.

The essential feature of the enciphered tag approach is that at the end of the record a tag appears which identifies the compartment from which the record was drawn. This compartment when deciphered can be compared with the access privileges of the user to determine whether the requested record should be passed on to the user. The principle of design is such that the tag cannot be forged in any way by a malicious user. It is assumed that the espionage agent cannot encrypt the record without the key. The simple encryption algorithm here is intended to illustrate the scrambling/descrambling program for purposes of studying timing and sizing of the guard. Subsequently, more advanced encryption algorithms will be used that will deny access for any period of decades, or even centuries.

The following points result from the assumption that the espionage agent cannot encipher the record when denied access to the key:

- Since the checksum is computed on the enciphered record, the espionage agent cannot compute the checksum. The agent can guess at it, but chances of guessing right are only 1 in 2^{32} .
- If the agent falsifies either the checksum or the record, such falsification will be detected by the guard when the calculated checksum is compared with that contained in the tag.
- Since the compartment identification is enciphered by combining it with the checksum, the agent cannot find out what the compartment is, and, further, cannot forge the compartment because it is both enciphered and has a checksum.

5.6.1 Key Initialization. The key is passed from the access control center to the exit guard. It consists of a string of 52 characters, as follows:

- Characters 1 through 40 equal all letters (no duplicates), all numbers (no duplicates), space, and special characters (any three).
- Characters 41 through 46 equal six-digit number which is a key to start a random number generator.
- Characters 47 through 52 equal 16 ones and zeros. A one indicates data access for this compartment.

5.6.2 Tagging Process. The tagging process consists of five steps, as follows:

1. Generate an 8-bit random number, RN.
2. Store RN in the tag.

3. Using temporary storage, encrypt the record as follows: for each character (8 bits), search the translation table for a match, If a match is found, replace the character with the index of the search. Increment RN. Logical exclusive OR the translated character with the random number table as indexed by RN.
4. Checksum the encrypted record and store in the tag.
5. Using the least significant 8 bits of the checksum as an index to the random number table, logically exclusive or the random number and store in the compartment.

5.6.3 Typical Record Tag. Figure 23 shows a diagram of a typical record. It is comprised of 16-bit words shown at the top of the diagram as Bit Positions 0 through 15.

There are N words in the record. The 0 position contains the number of words in the record, N. The last three words in the record contain the necessary information. The random number is contained in the low byte of word N -4. The compartment is stored in position N -3, and the checksum is contained in two words, Positions N -2 and N -1.

5.6.4 Detagging Process. The detagging process proceeds in six steps, as follows:

1. Fetch RN from the tag.
2. Encrypt record as described in Step 3 of the tagging process.
3. Computer checksum of the encrypted record.
4. Using the technique described by Step 5 of the tagging process, fetch the compartment.
5. Logical exclusive OR the key compartment and the compartment from 4 and store the result in the compartment.
6. If the checksums from the tag and result of 3 equal, and if compartment equals 0, the tag is correct.

5.7 Detailed Flow Diagrams - Query Processing. This section contains the detailed flow diagrams corresponding to the top level flow in Section 5.4 dealing with Query Processing. Each of the six blocks of Figure 20 will be discussed in more detail.

A subroutine named CCNTL acts in the capacity of supervisor for the Query Processor. A flow diagram of CCNTL is shown in Figure 24, as well as a correlation between it and the top level diagram Figure 20.

5.7.1 Accept Request. As stated in Section 5.4.2 the purpose of this block is to initialize the necessary tables and message buffer pointers for the generation of the reverse Polish code, which is the intermediate language. A detailed flow of the initialization function is given in Figure 25.

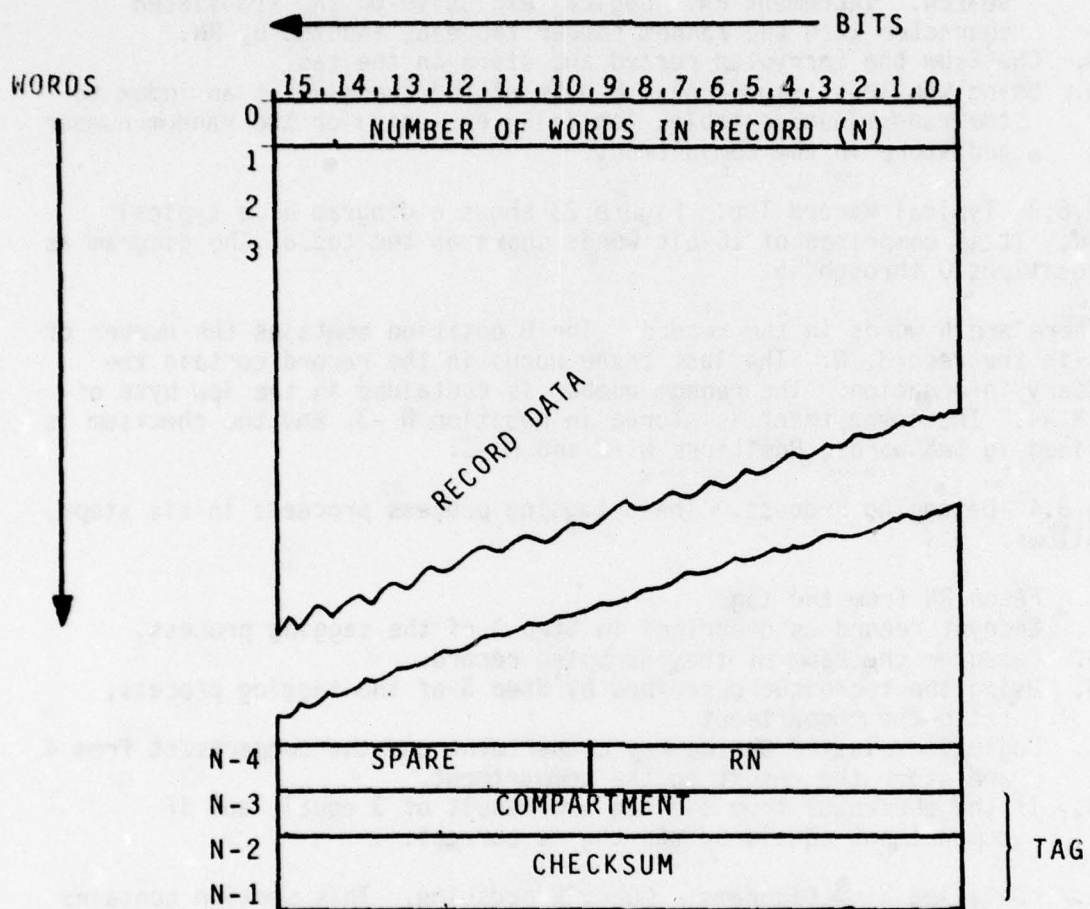


Figure 23
TYPICAL RECORD TAG

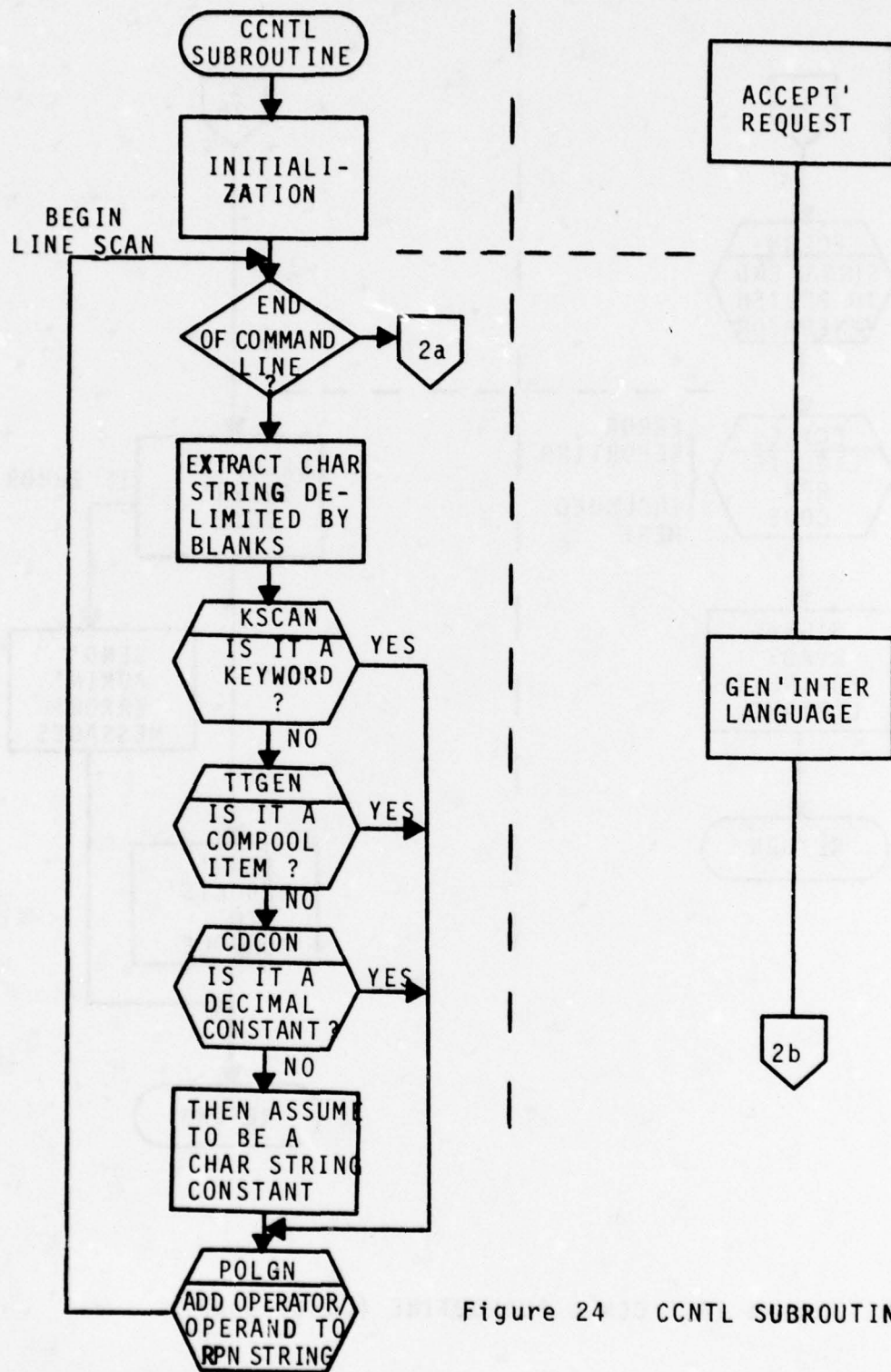


Figure 24 CCNTL SUBROUTINE

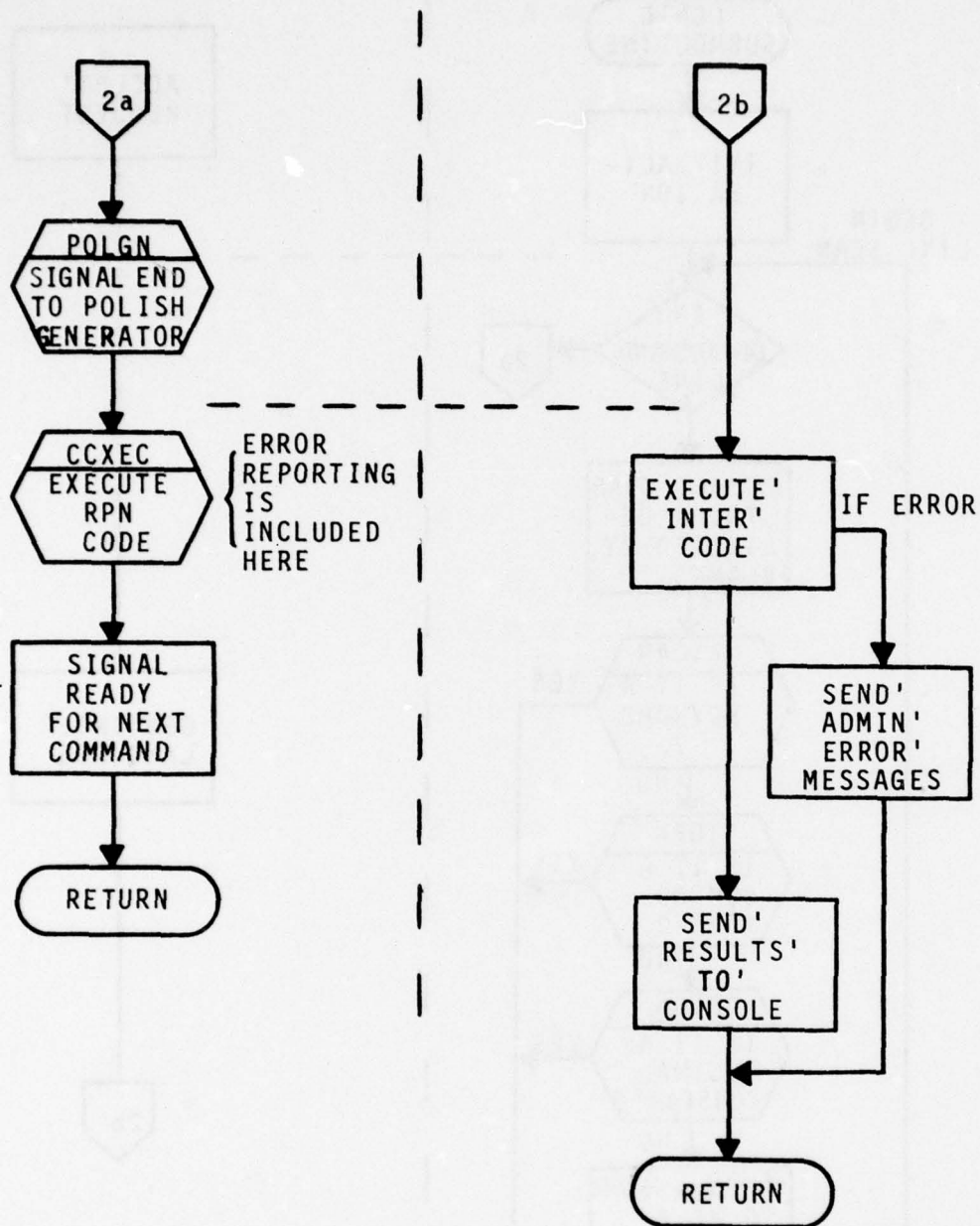


Figure 24 CCNTL SUBROUTINE (Continued)

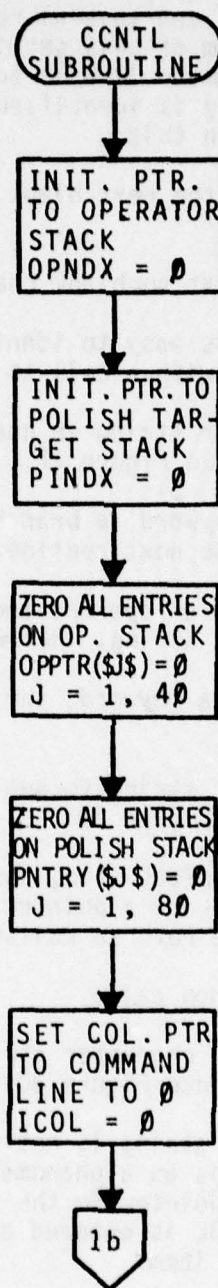


Figure 25 INITIALIZATION PHASE

5.7.2 Generate Intermediate Language. Generation of the reverse Polish code is a multistep process, and several routines are used to simplify the operation. A flow diagram of this section of the CCNTL can be found in Figure 26. First, the command line is scanned from left to right and each successive character string is identified and processed individually. Two Jovial operations aid in this:

BLNK - which searches for the next blank character in a command line.

NBLNK - searches for the next nonblank character in a command line.

With these two operations, it is easy to identify a character string and begin processing. This begins with a call to the following routine:

KSCAN - checks the character string in question to see if it is a keyword. Reference Figure 27.

If the character string is a keyword, a branch is taken to enter the keyword on the Polish string via the next routine.

POLGN - accepts an operator or operand and correctly places it into the Polish target string. Reference Figure 28.

If the character string is not a keyword, the following routine is called:

TTGEN - Compare a character string to see if it is a valid COMPOOL item. Reference Figure 29.

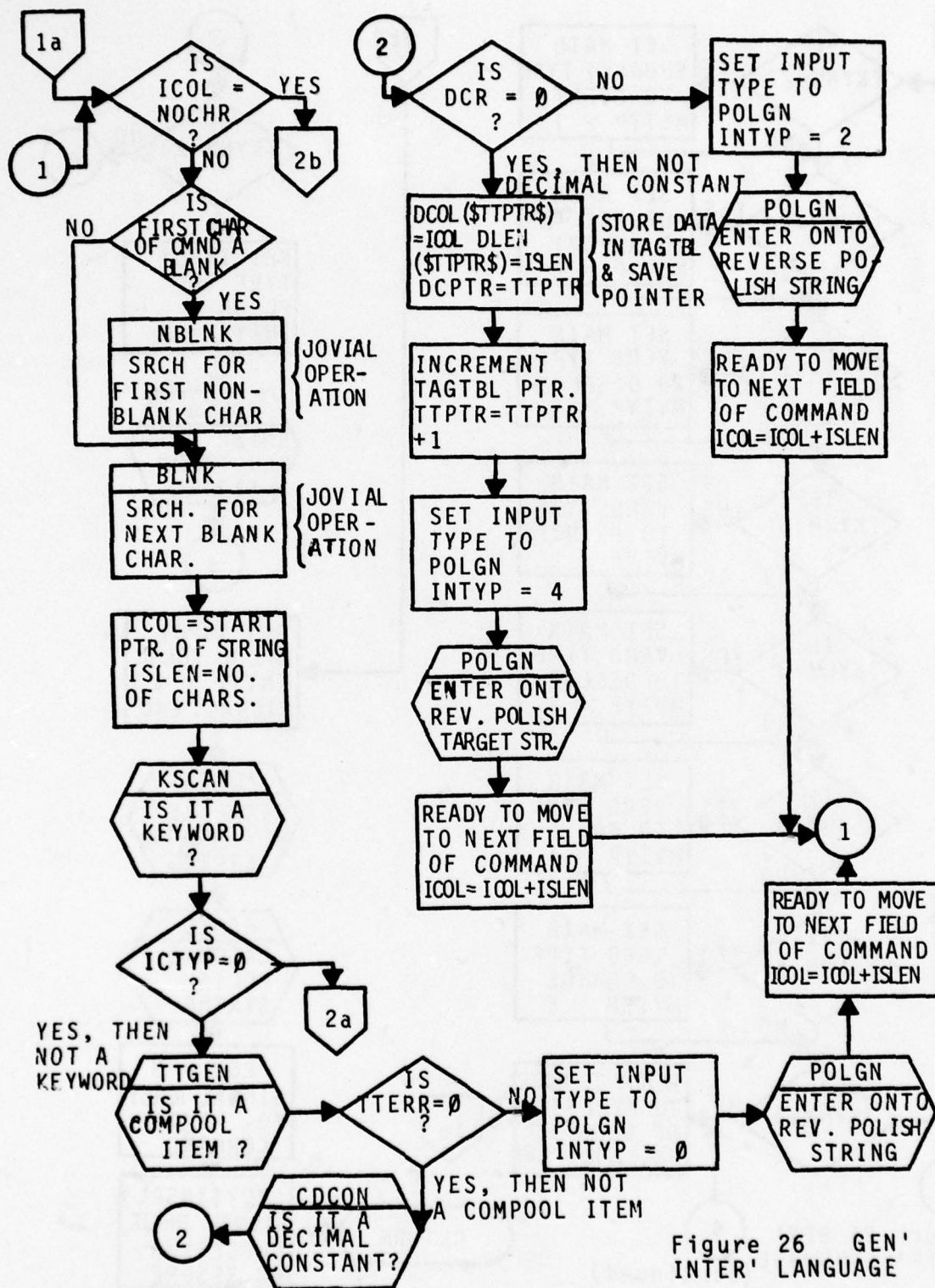
If the character string is a COMPOOL item, then the attributes of that item are stored in a table, TAGTBL, and a pointer to that entry in the table is saved and entered onto the reverse Polish string via POLGN.

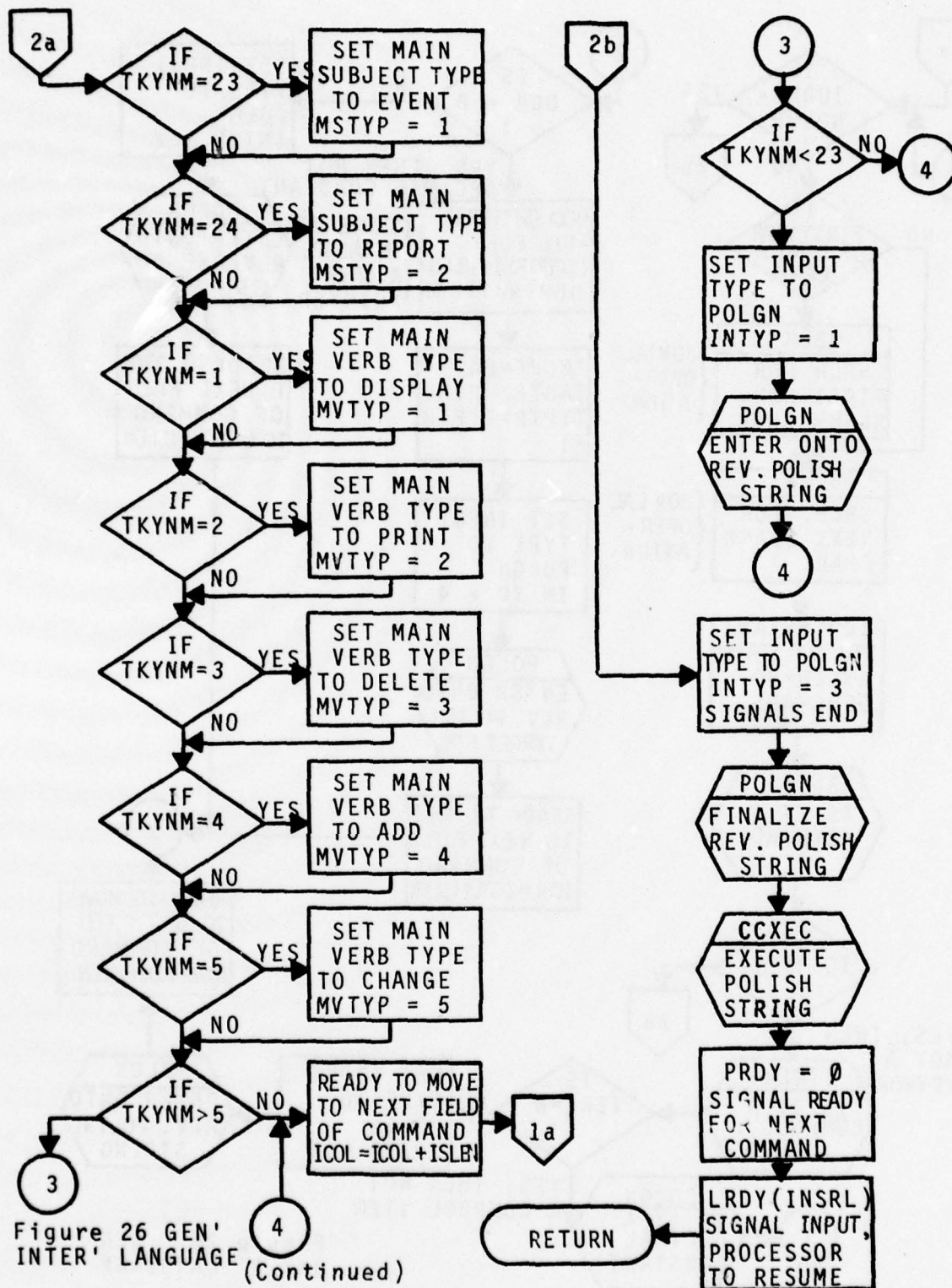
If it is not a COMPOOL item, then call:

CDCON - Check to see if the character string is a decimal constant. Reference Figure 30.

In the case that the character string is not a decimal constant, it is assumed that the character string is an alphanumeric constant to be compared. The length and the column pointer to the string are stored in the TAGTBL and the pointer to the TAGTBL is entered onto the reverse Polish string via POLGN as with a COMPOOL item.

If the character string is a decimal constant, it is converted to binary and stored in the TAGTBL, with the pointer again to be entered on the reverse Polish string via POLGN.





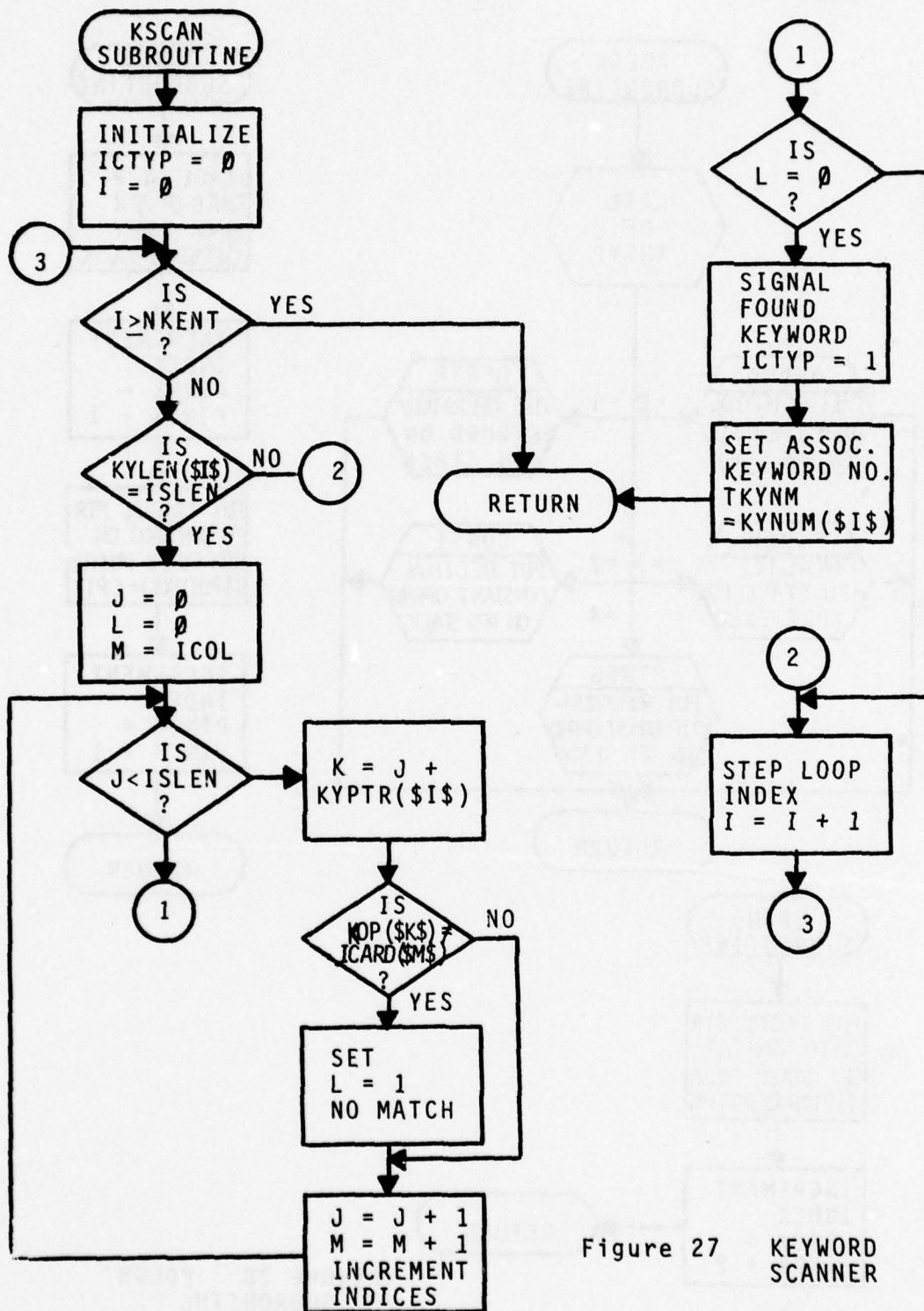


Figure 27 KEYWORD SCANNER

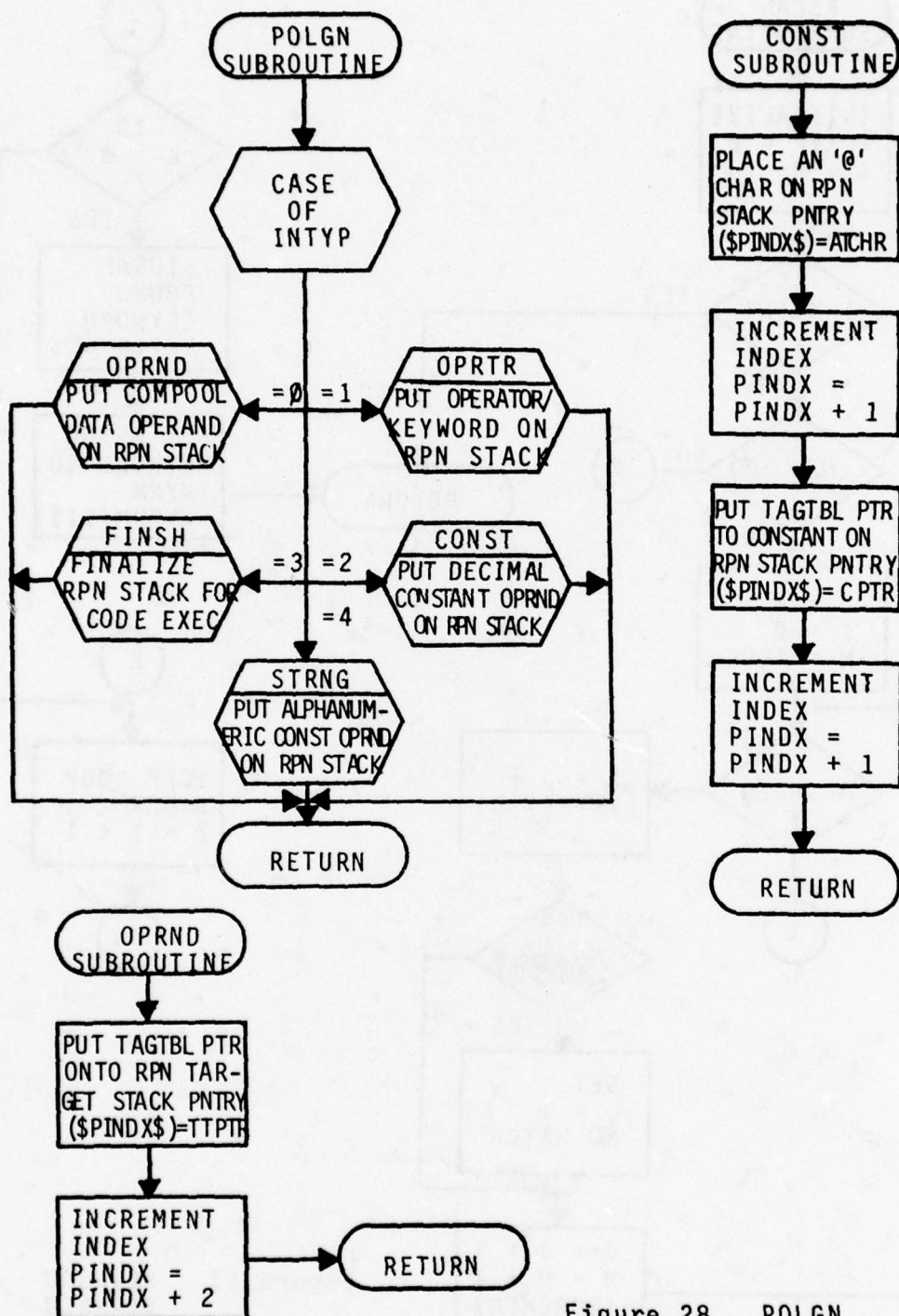


Figure 28 POLGN
SUBROUTINE

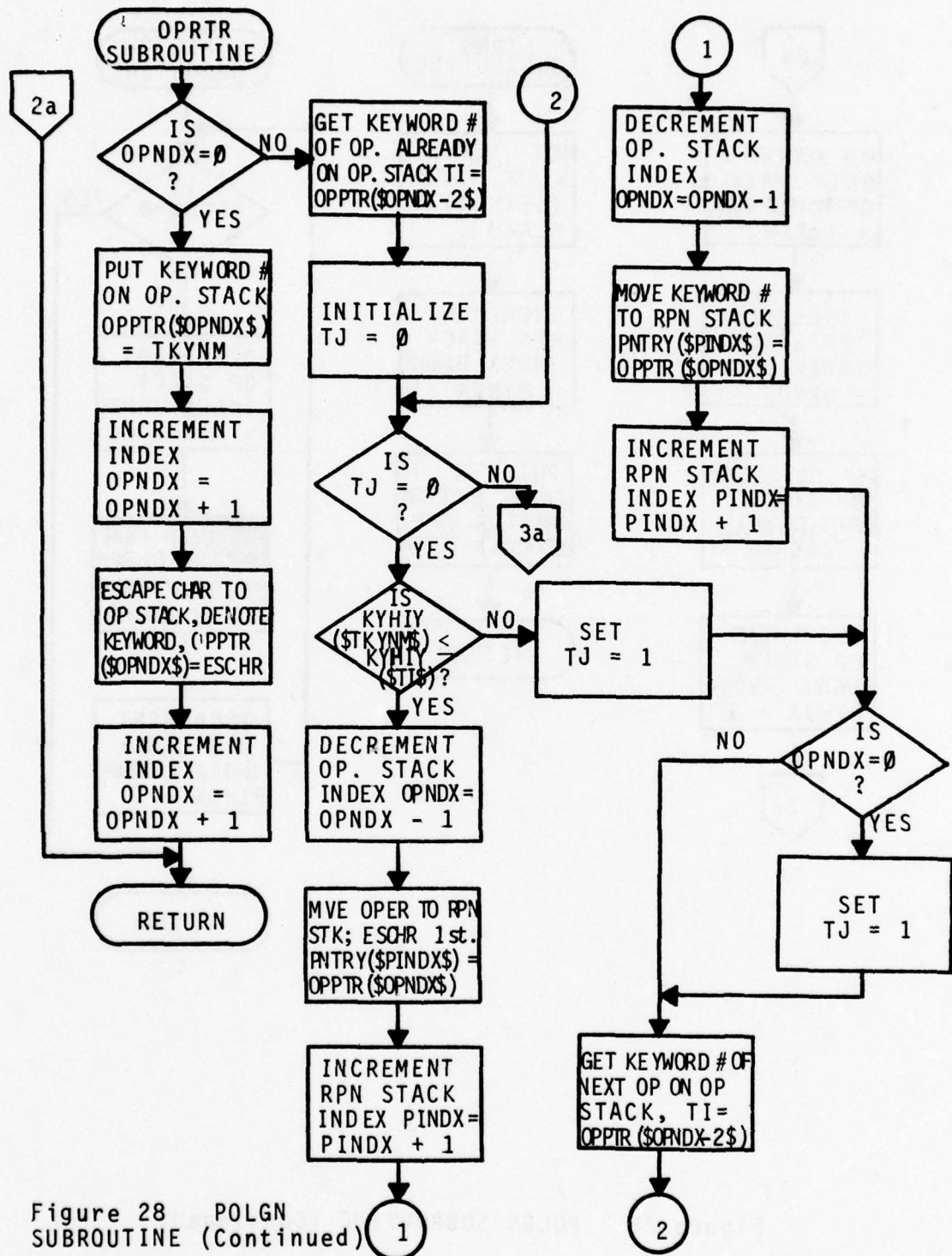


Figure 28 POLGN SUBROUTINE (Continued)

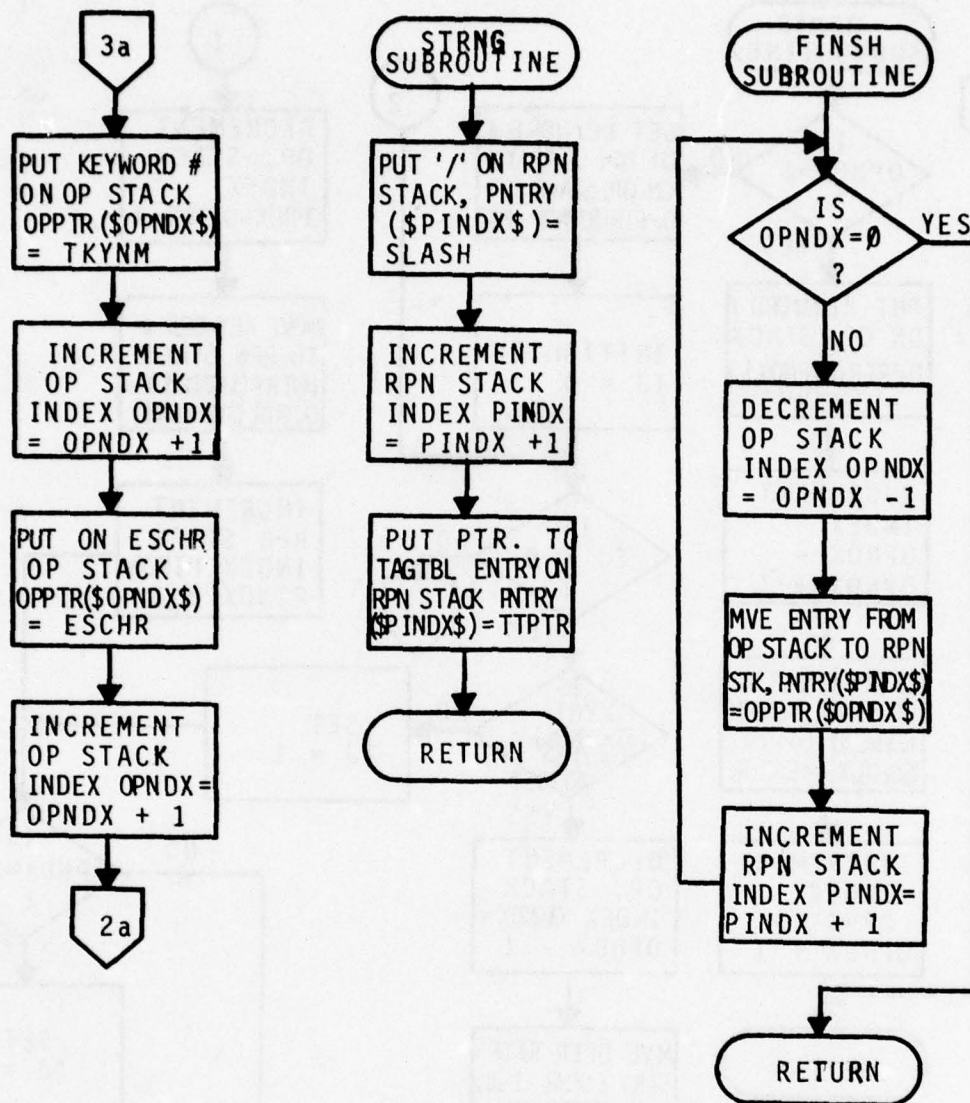


Figure 28 POLGN SUBROUTINE (Continued)

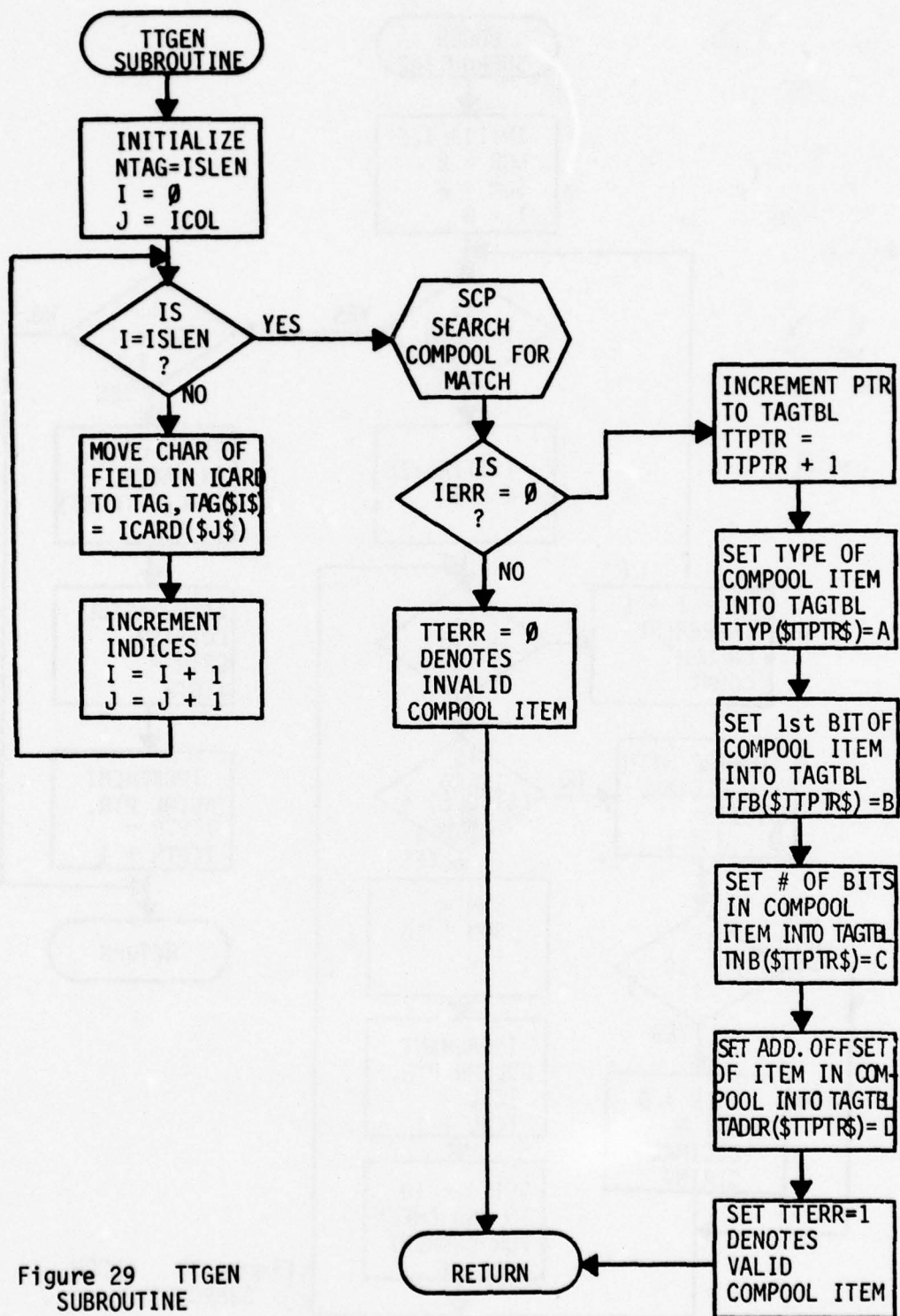


Figure 29 TTGEN
SUBROUTINE

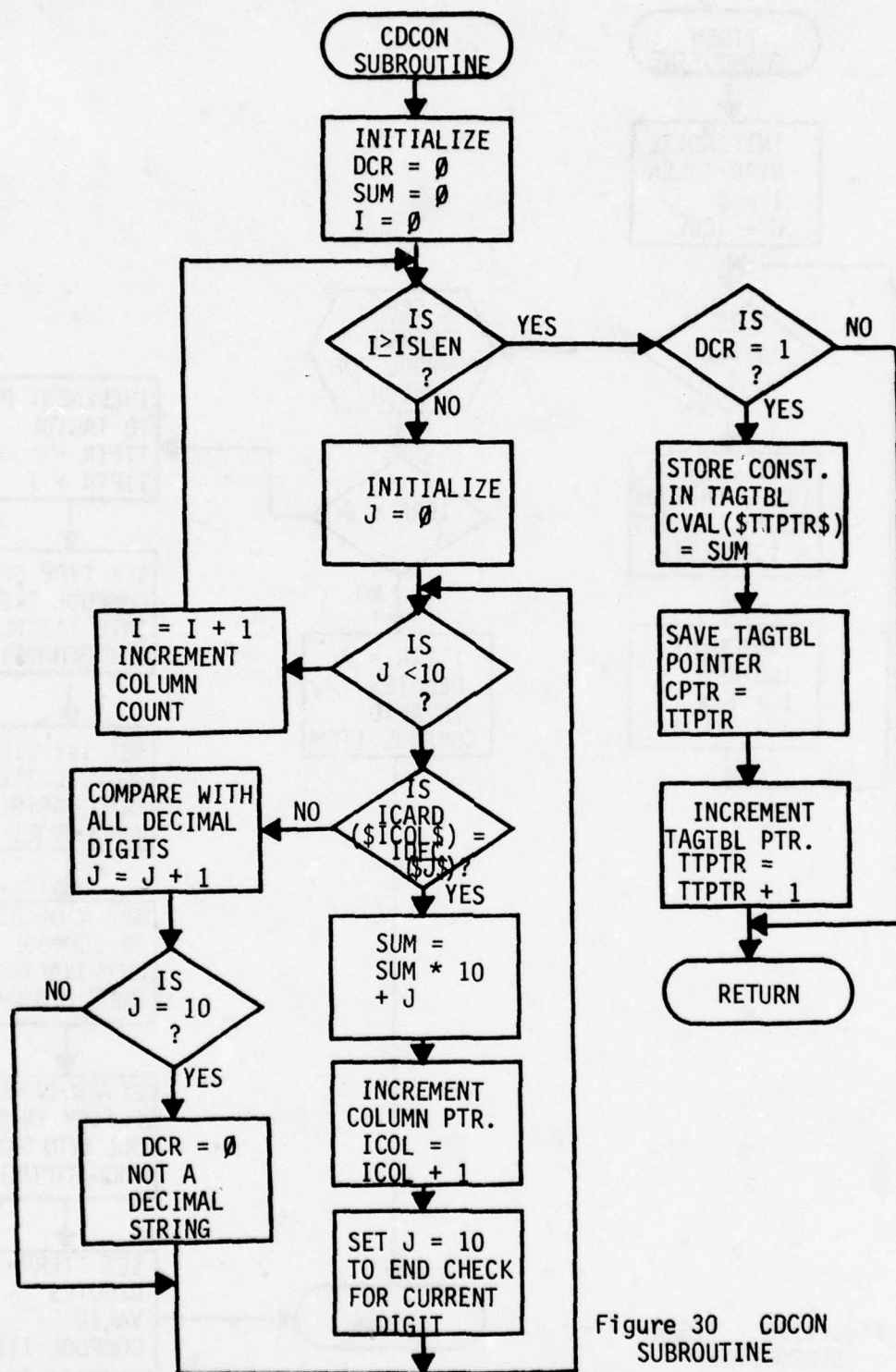


Figure 30 CDCON
SUBROUTINE

Thus, each field of the command line fits into one of the following categories; keyword, compool item, decimal constant or character string (alphanumeric) constant. After the whole command line has been processed in this manner, one last call is made to POLGN to put the reverse Polish code in its final form before execution.

5.7.3 Code Execution. This section deals with the code execution routine, CCXEC, which is described in Paragraph 5.4.6. In addition, CCXEC also carries out the functions of error reporting discussed in Sections 5.4.4 and 5.4.5, although they are not fully implemented at this time, as well as the SEND RESULTS TO CONSOLE function dealt with in 5.4.7. A detailed flow of CCXEC is shown in Figure 31.

First, the subject of the command, event or report, is used to set the disk sector base and the record count for the code execution loop. Each record is read off of the disk into memory and the RPN string is executed using that record to yield a true or false result. If true, the proper routine is called, determined by the verb type MVTYP, to perform the desired operation on the current record. The next disk record is read in and the same sequence is repeated until all records have been read.

The actual execution of the RPN string takes place as follows. Each entry in the RPN string is handled separately. A check is made to see if the entry is an operator, which is denoted by preceding the keyword number on the stack with an escape character. Once the existence of the operator is determined, the keyword number is used to identify the correct routine to carry out the appropriate operation. All necessary operands have already been placed on the working stack by nature of the RPN string and the result of the operation is returned to that stack.

In a similar manner, the decimal constants are denoted by an '@' character which is followed by a pointer to the actual constant in the TAGTBL. The constant is placed on the working stack and control proceeds to the next entry on the RPN string.

For a character string, a slash character precedes a pointer to an entry in the TAGTBL which contains the length of the string and its starting column in the command line in the table ICARD. The data is placed on the working stack and a flag indicate string mode is set. This ensures proper handling of the string during its operation. Control then moves on to the next RPN entry.

If none of the special characters are recognized, the entry is just a pointer to the TAGTBL, which contains the attributes of a compool item. The attributes are used to place that compool item onto the working stack. Control again returns to handle the next entry on the RPN stack.

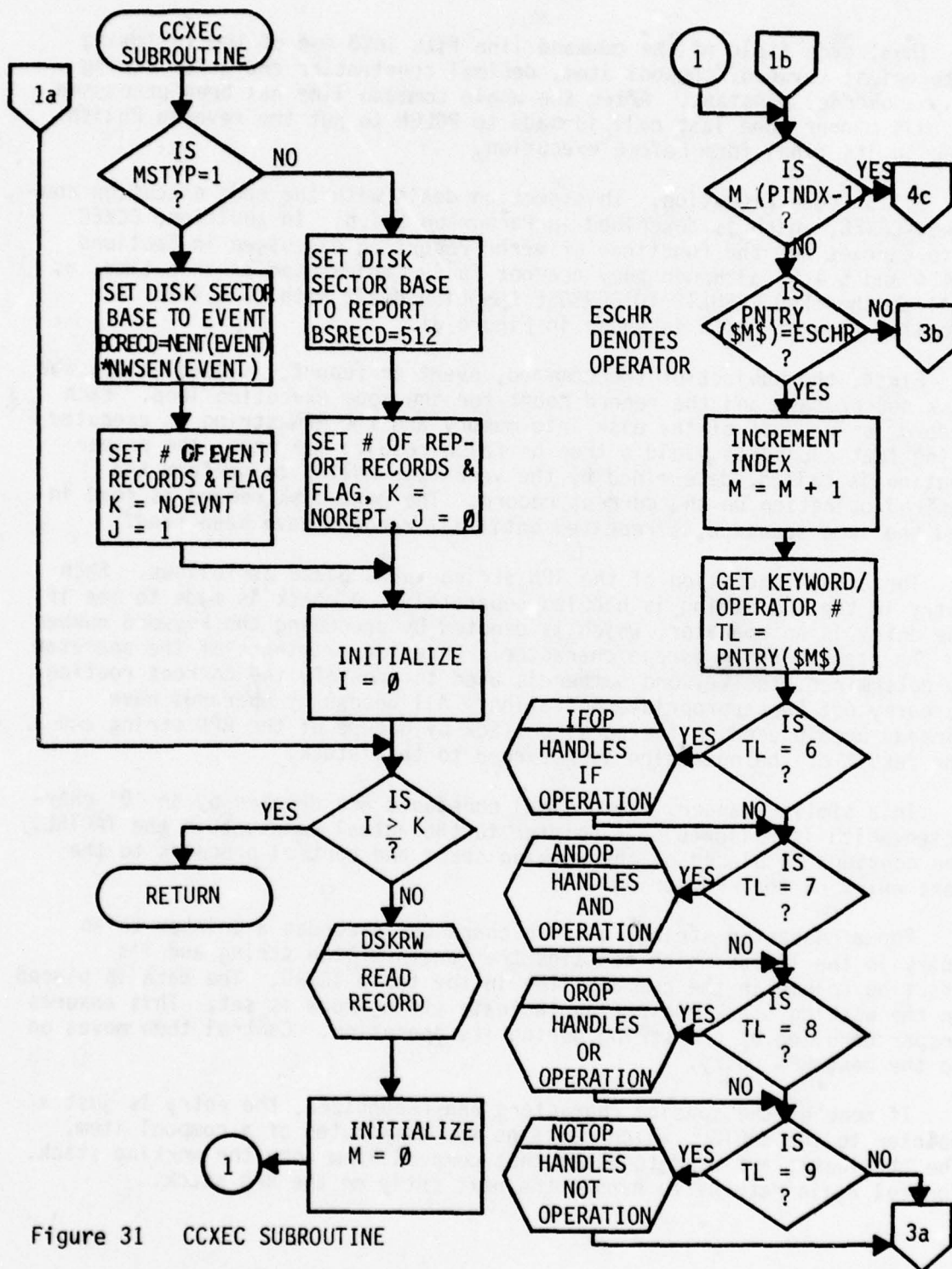


Figure 31 CCXEC SUBROUTINE

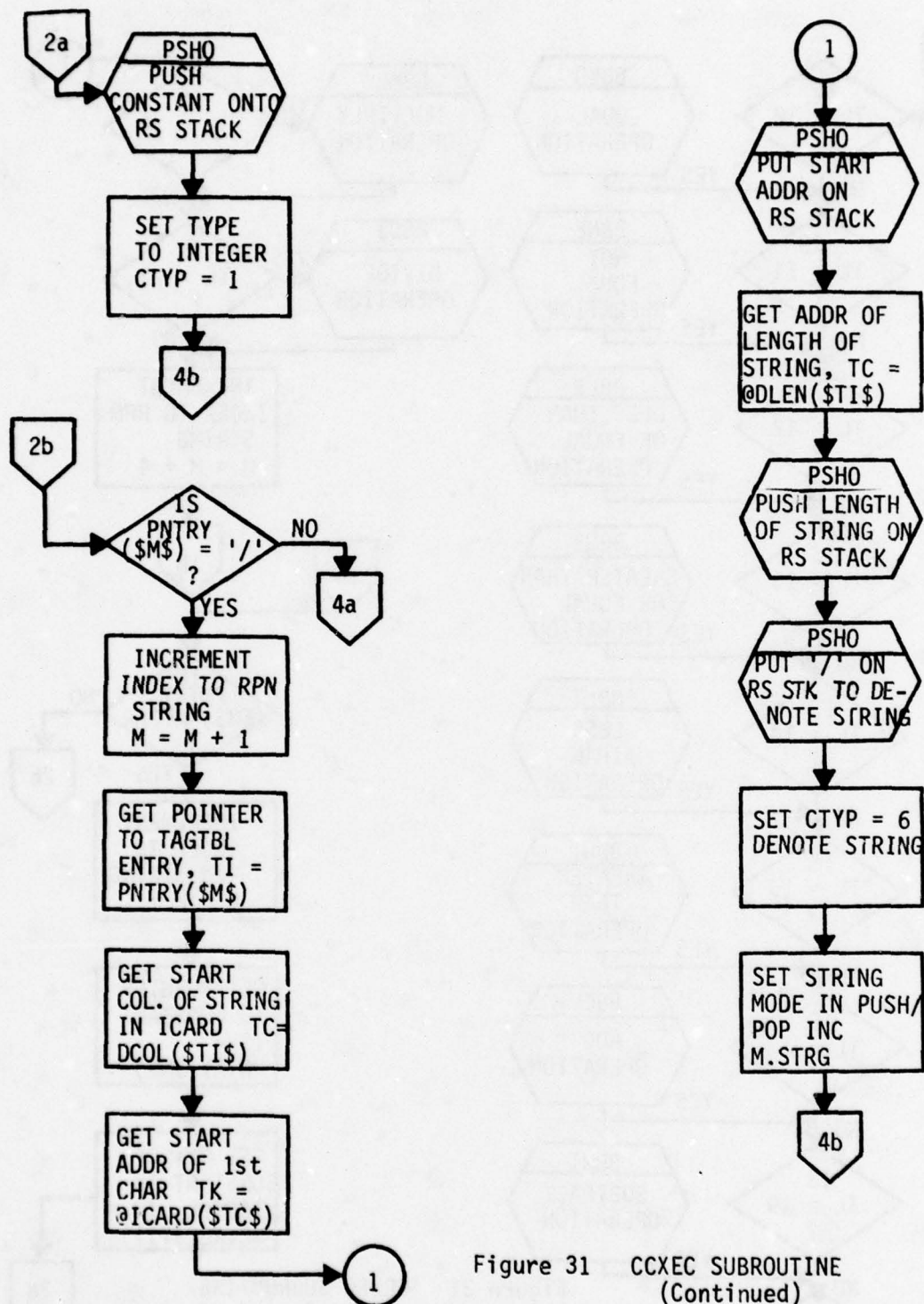
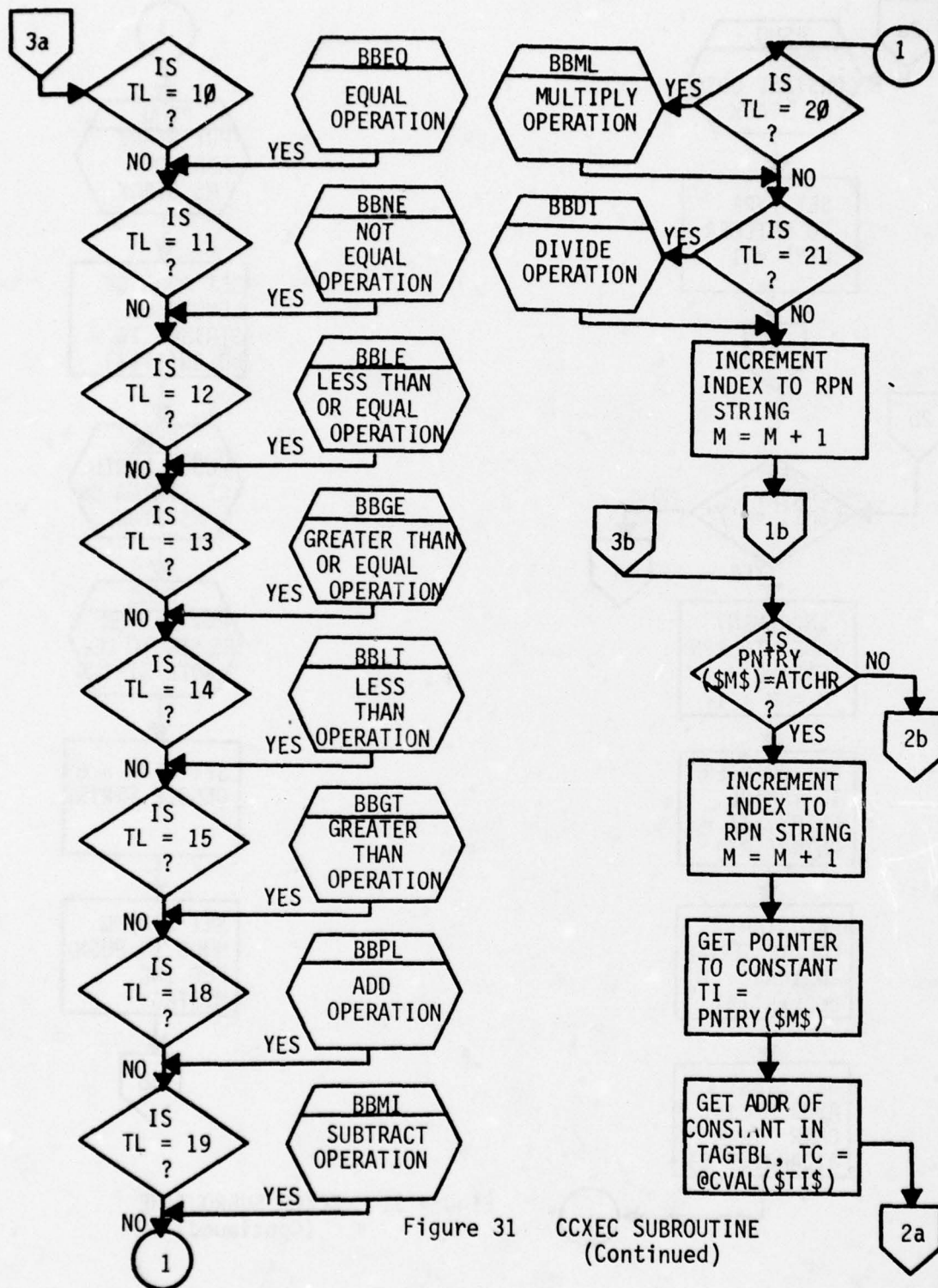


Figure 31 CCXEC SUBROUTINE
(Continued)



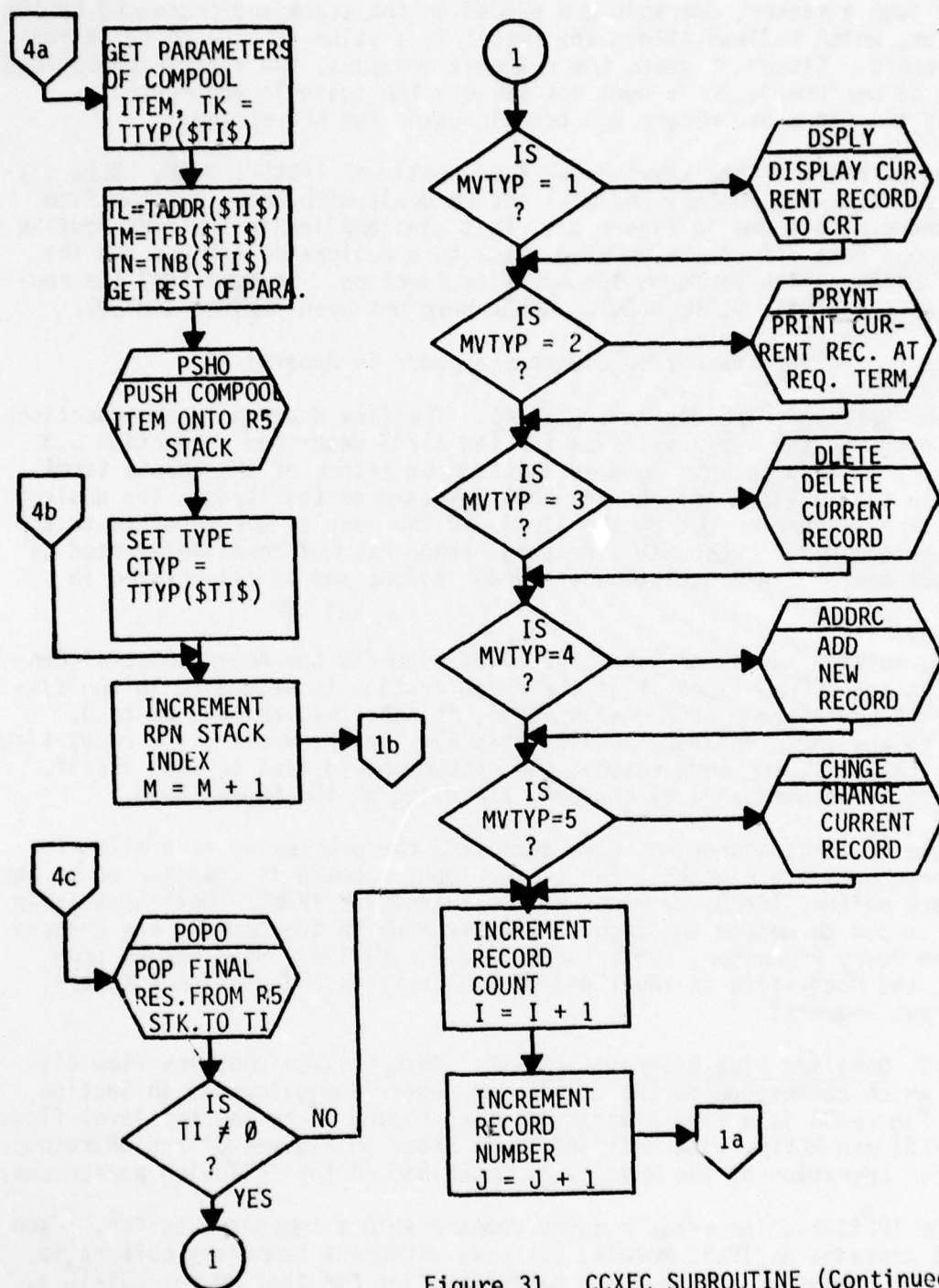


Figure 31 CCXEC SUBROUTINE (Continued)

In such a manner, operands are placed on the stack and processed by the operator, which follows them. The result is a value of true or false for each record. Either it meets the criteria and thus, the desired operations should be performed, or it does not satisfy the criteria and control returns to read a new record and test it using the RPN string.

The purposes of the keyword/operator routines, (ANDOP, OROP, BBLE, ... etc.) are self-explanatory and will not be dealt with here, but the flow diagrams can be found in Figure 31. This also applies to the POPO routine which pops data off of the working stack to a designated address and the PSHO routine, which performs the opposite function. In addition, the routines DSPLY, PRMNT, DELETE, ADDR, CHNGE have not been implemented yet.

The coding for these flow diagrams appears in Appendix A.

5.8 Detailed Flow Diagrams - 11/45. The flow diagram in this section corresponds to the top level flow for the 11/45 described in Section 5.3. The routine INP45 accepts command inputs from either of the remote terminals via the LSI-11's or from the LA36 keyboard on the 11/45. The desired processing is carried out by the 11/45 and the results are returned to the calling terminal. Presently, the card reader has not been implemented as an input source. A description of INP45 follows and is illustrated in Figure 32.

The initialization of the 11/45 takes place in the Access Control Center routine, ACCPM, since it is the first routine to be called in the system start-up. Before ACCPM calls INP45, it sets the variable GO to 0, which causes INP45 to loop, polling possible input sources via a ready flag table, LRDY. If for some reason, the system should need to stop itself, this can be accomplished by changing the value of the GO variable.

Once an input source has been detected, the processing is similar for all three possible sources. First, the input command is transferred to the RPN work buffer, ICARD, by means of the subroutine TRANC. Next a variable INSRC is set to denote the input source from which the command was entered and the Query Processor, CCNTL subroutine, is called. Upon return from CCNTL, the ready-flag is reset and control returns and continues to poll the input sources.

5.9 Detailed Flow Diagram - LSI-11. This section contains flow diagrams which correspond to the LSI-11 top level flow discussed in Section 4.2. Figure 33 is a flow diagram relating Figure 18 to the top level flows for IPLSI and RCVIP, with detailed flows shown in Figures 34 and 35 respectively. Operation of the modules is described in the following paragraphs.

The IPLSI routine reads a query command into a temporary buffer. Each LSI-11 contains an IPLSI module, but uses different temporary buffers to store the command. The ready or handshake flag for that unique LSI-11 is set to notify the 11/45 that a command is ready for processing. Control

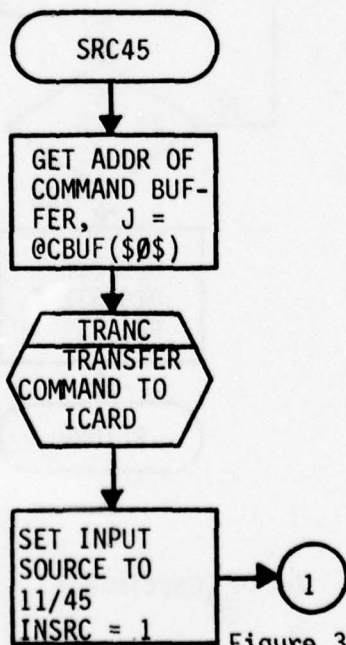
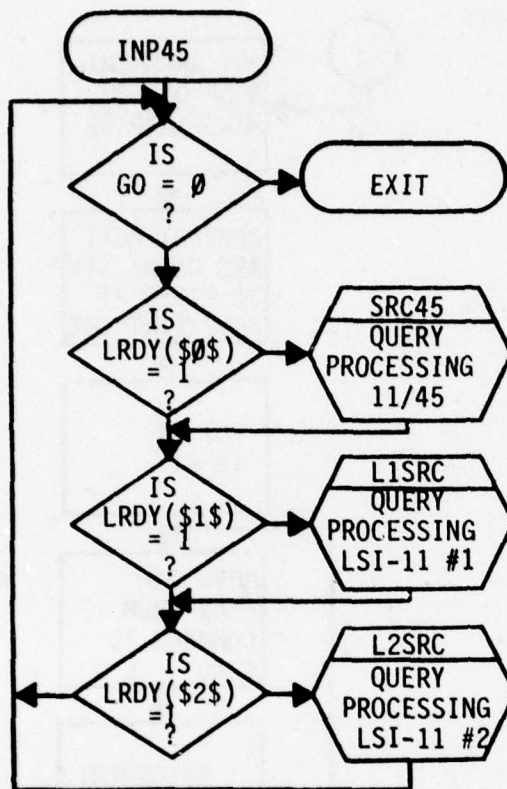
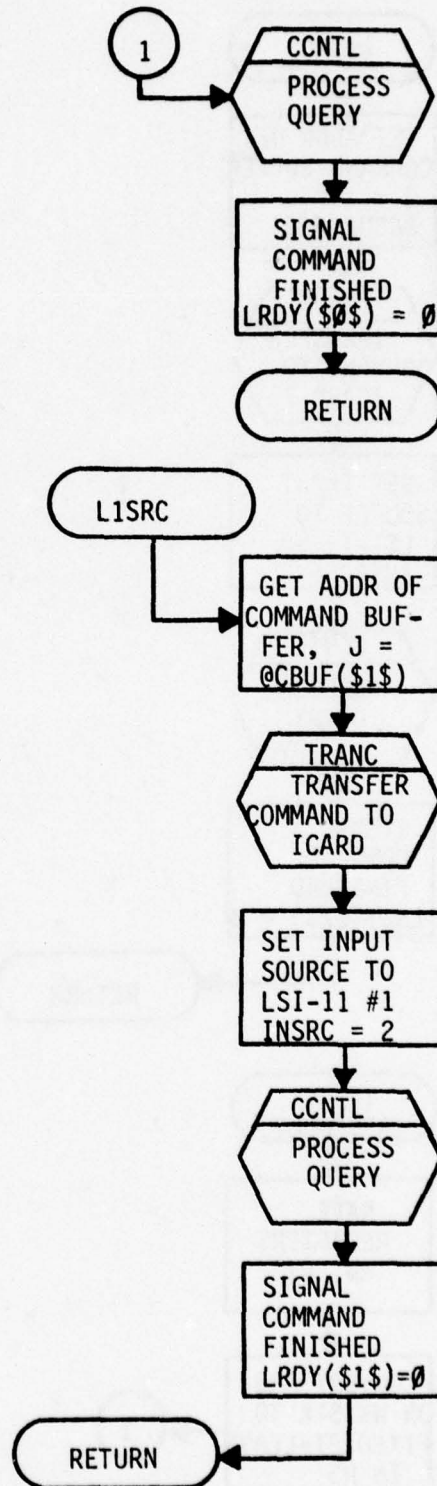


Figure 32

INP45



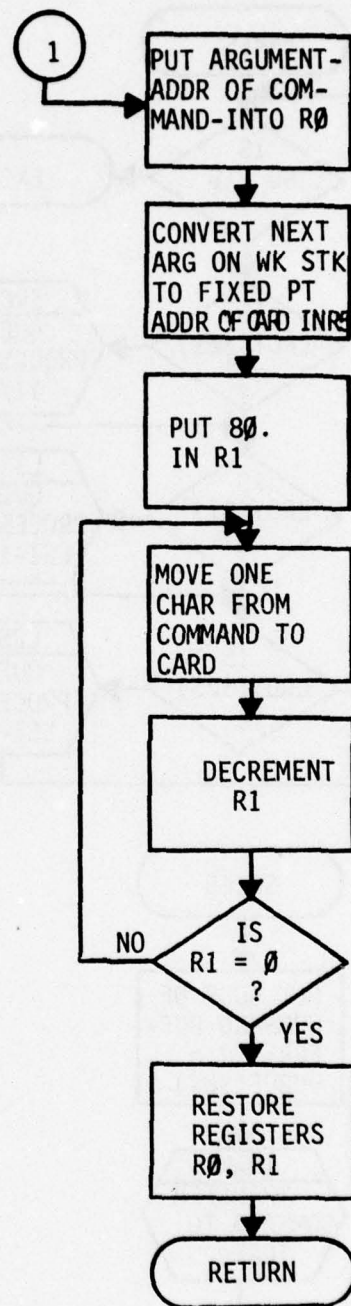
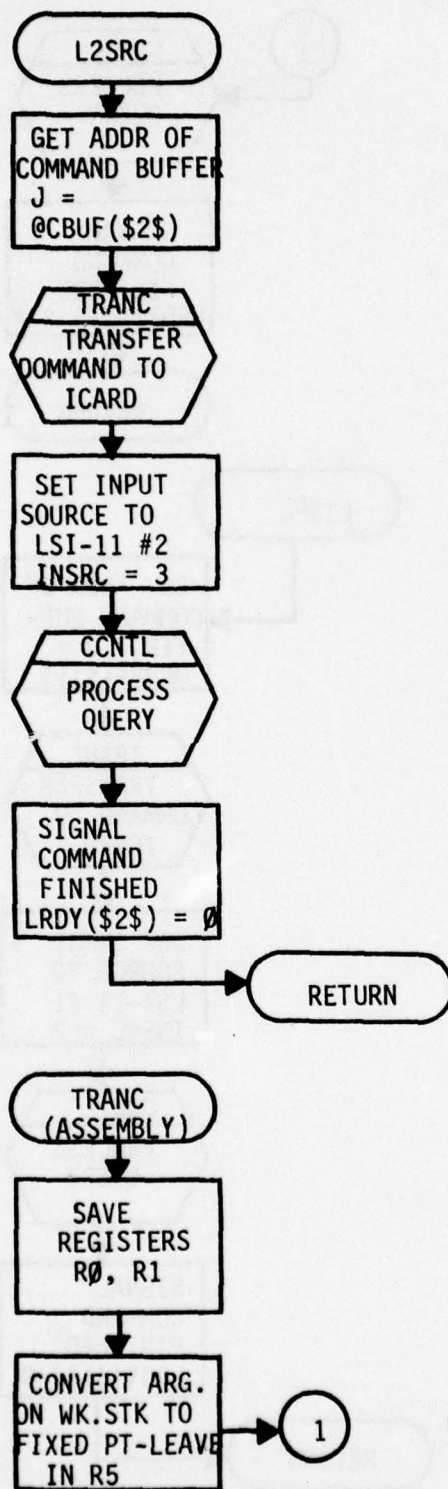


Figure 32 INP45 (Continued)

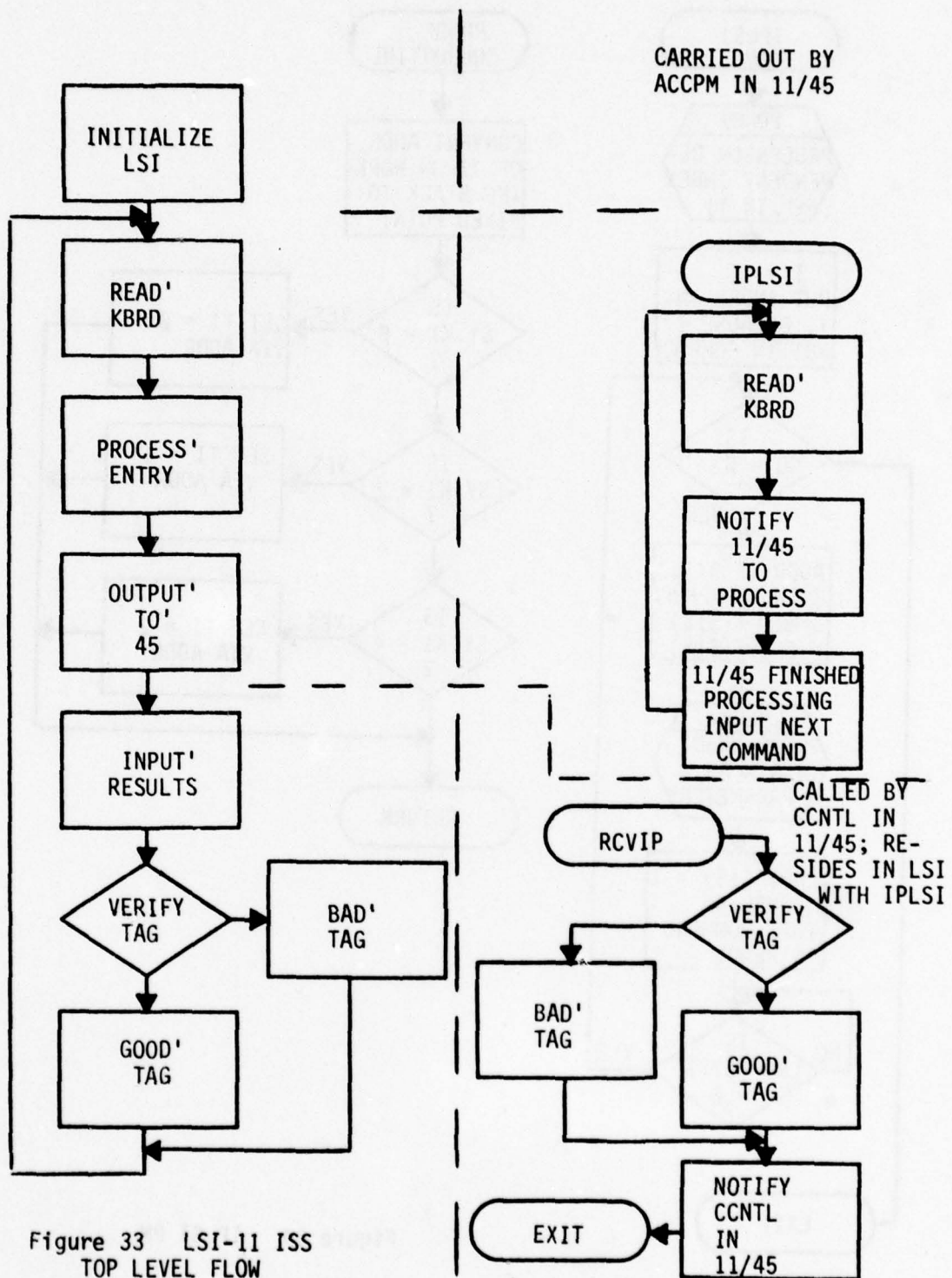


Figure 33 LSI-11 ISS
TOP LEVEL FLOW

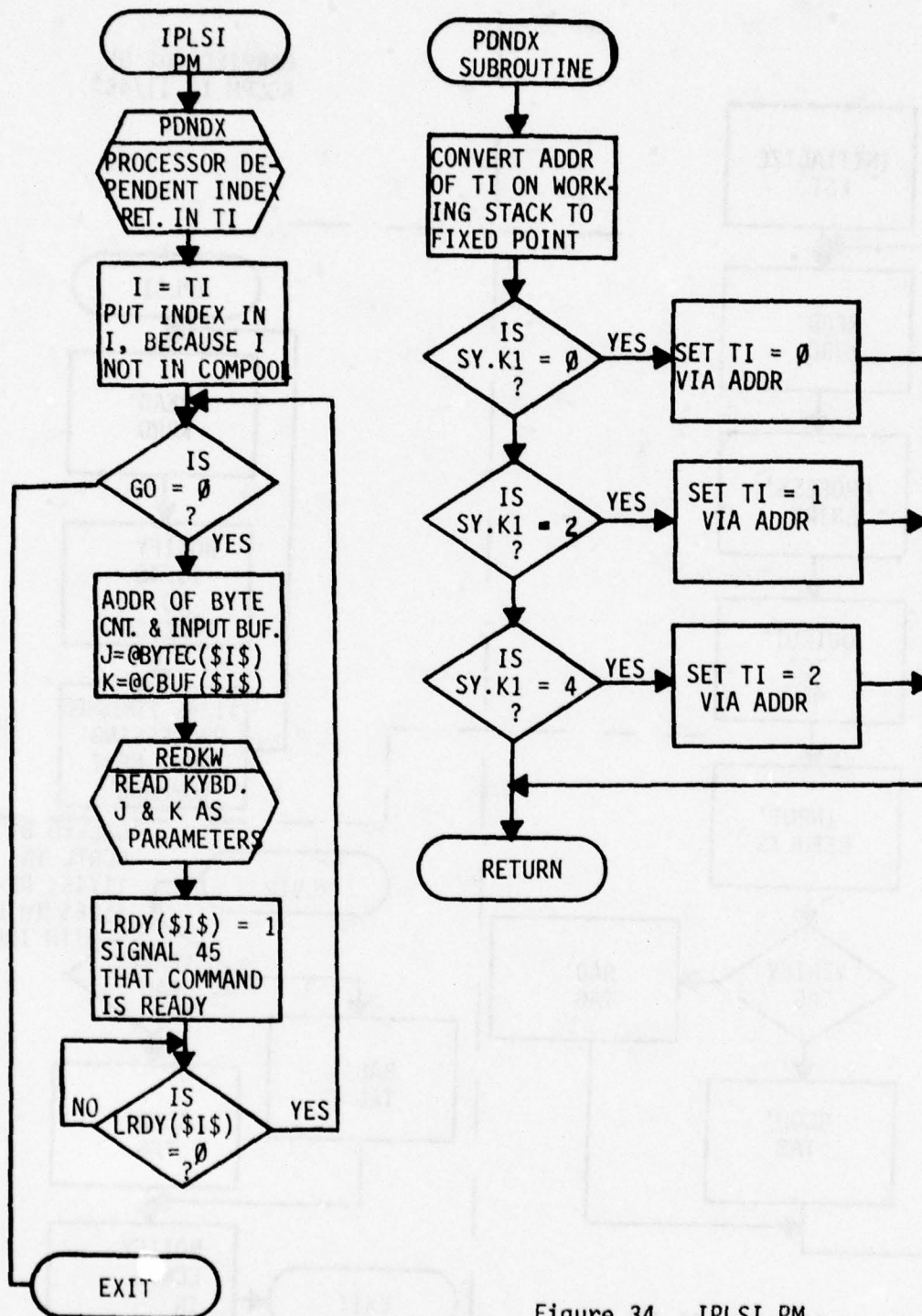


Figure 34 IPLSI PM

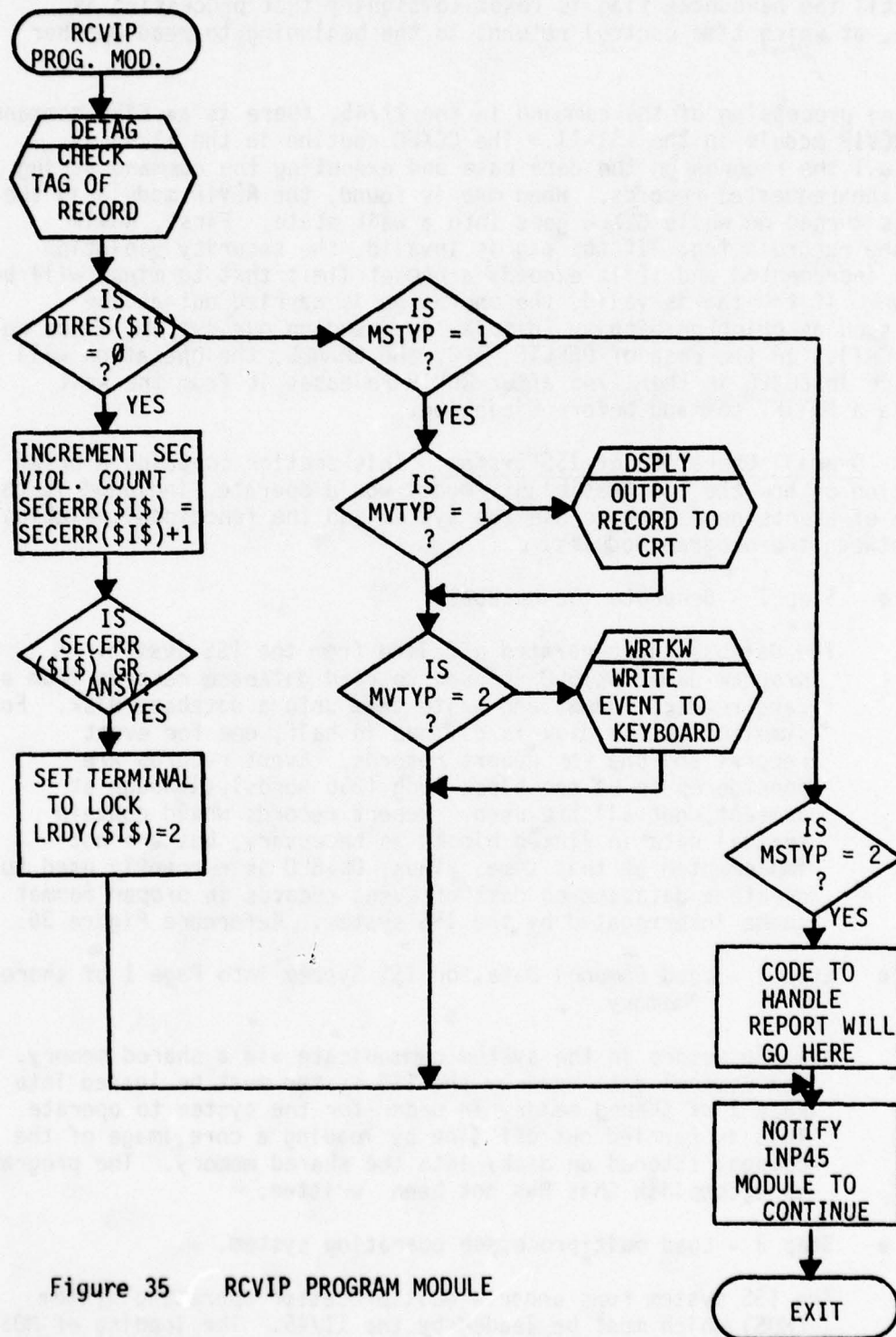


Figure 35 RCVIP PROGRAM MODULE

loops until the handshake flag is reset to signify that processing is complete, at which time control returns to the beginning to read another command.

During processing of the command in the 11/45, there is an EXEC command to the RCVIP module in the LSI-11. The CCXEC routine in the 11/45 is reading all the records on the data base and executing the command string to find the requested records. When one is found, the RCVIP module in the LSI-11 is turned on while CCXEC goes into a wait state. First, RCVIP checks the record's tag. If the tag is invalid, the security violation count is incremented and if it exceeds a preset limit that terminal will be shut down. If the tag is valid, the operation is carried out at the LSI-11, such as print or display (display not used on our system, since we have no CRT). In the case of DELETE, ADD, and CHANGE, the operation will take place in CCXEC in the 11/45 after RCVIP releases it from the wait state via a NOTIFY command before finishing.

5.10 Overall Operation of ISS System. This section contains a brief description of how the ISS feasibility model would operate, included is the sequence of events necessary to use the system and the functional relationships between the program modules.

- Step 1 - Generate the database.

The database is generated off line from the ISS system. A program named DK1BLD is used to read database records from a card reader, format and write them onto a database disk. For simplicity, the disk is divided in half, one for event records and one for report records. Event records are considered to be one block long (256 words) although at present, not all are used. Report records would contain textual data in linked blocks as necessary, but are not implemented at this time. Thus, DK1BLD is currently used to create a database on disk of event records in proper format to be interrogated by the ISS system. Reference Figure 36.

- Step 2 - Load Compool Data for ISS System into Page 1 of shared memory.

All processors in the system communicate via a shared memory. The Compool data used by the ISS system must be loaded into Page 1 of shared memory in order for the system to operate. This is carried out off line by loading a core image of the compool (stored on disk) into the shared memory. The program to accomplish this has not been written.

- Step 3 - Load multiprocessor operating system.

The ISS system runs under a multiprocessor operating system (MOS) which must be loaded by the 11/45. The loading of MOS

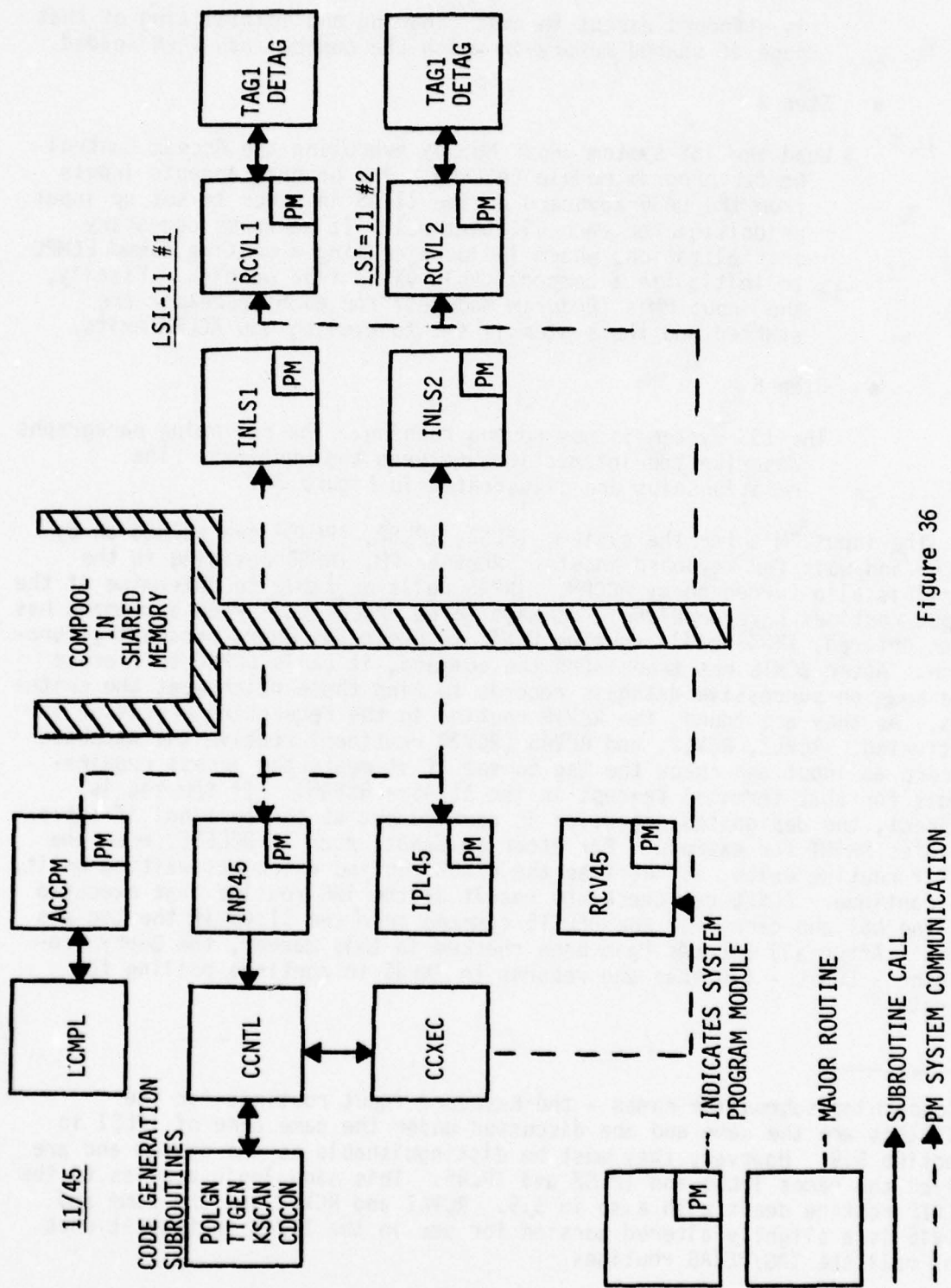


Figure 36

is standard except to omit clearing and initializing of that page of shared memory in which the compool has been loaded.

- Step 4

Load the ISS system under MOS by executing the Access Control Center program module (ACCPM). The program accepts inputs from the LA36 keyboard on the 11/45 in order to set up input priorities for each LSI terminal. It performs necessary initialization, which includes calling a routine named LCMPL to initialize a compool table via a file on disk. Finally, the input PM's (Program Modules) for each processor are started and the system is set to cycling and ACCPM exits.

- Step 5

The ISS system is now up and running. The following paragraphs describe the interactions between the routines. The relationships are illustrated in Figure 36.

The input PM's for the system, IPLS1, IPLS2, IPL45* are turned on by ACCPM and wait for keyboard inputs. Another PM, INP45 residing in the 11/45 is also turned on by ACCPM. INP45 polls a table to determine if the input routines have received a command to be processed. When a command has been entered, INP45 calls routine CCNTL to begin the Query processing function. After CCNTL has translated the command, it calls CCXEC to execute the code on successive database records to find those which meet the criteria. As they are found, the RCVIP routine in the requesting processor is activated. RCVL1, RCVL2, and RCV45 (RCVIP routines) receive the database record as input and check the tag to see if it meets the access requirements for that terminal (except in the 11/45 - RCV45). If the tag is correct, the designated operation is carried out at the terminal if appropriate, PRINT for example. For other commands, such as DELETE, when the RCVIP routine exits, it notifies the CCXEC routine which was waiting on it, to continue. CCXEC can check the result of the TAG routine that executed in the LSI and carry out the DELETE command from the 11/45 if the tag was good. After all records have been checked in this manner, the Query Processor - CCNTL - finishes and returns to INP45 to continue polling for inputs.

* Concerning subroutine names - the keyboard input routines for the LSI-11's are the same and are discussed under the same name of IPLSI in Section 5.9. However, they must be distinguishable to the system and are given the names IPLS1 and IPLS2 and IPL45. This same logic applies to the PCVIP routine dealt with also in 5.9. RCVL1 and RCVL2 are the same and RCV45 is a slightly altered version for use in the 11/45 in that it does not call the TAG/DETAG routines.

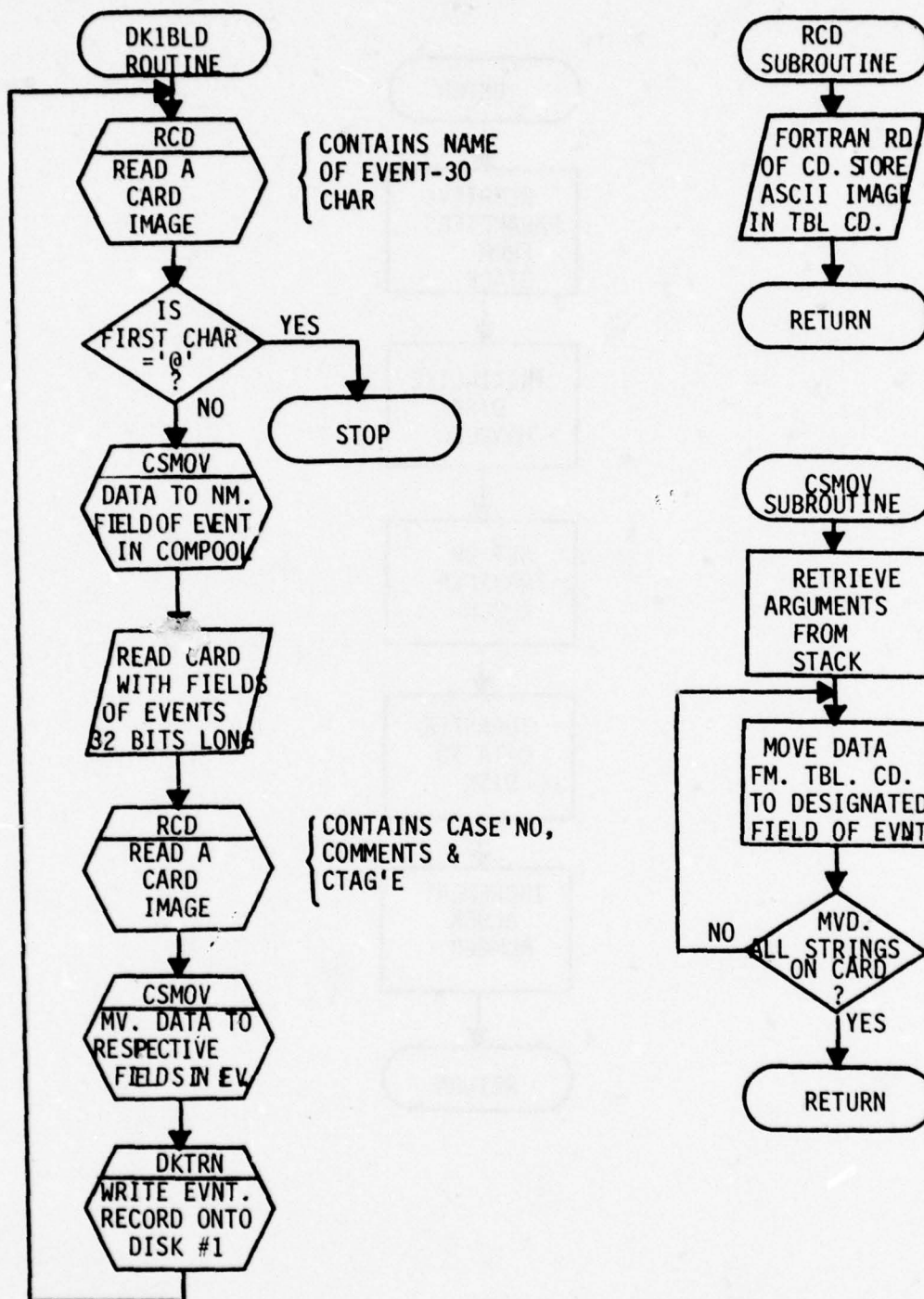


Figure 37 DK1BLD ROUTINE

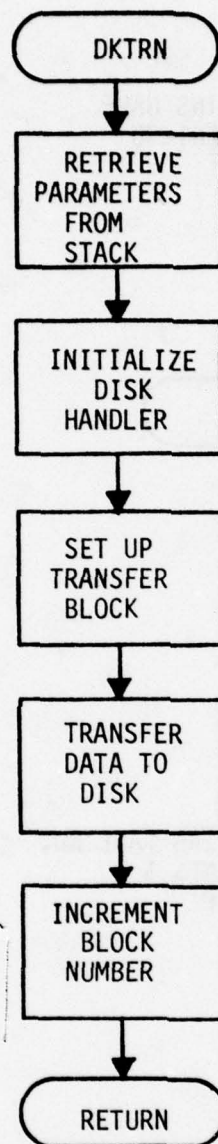


Figure 37 DKIBLD ROUTINE (Continued)

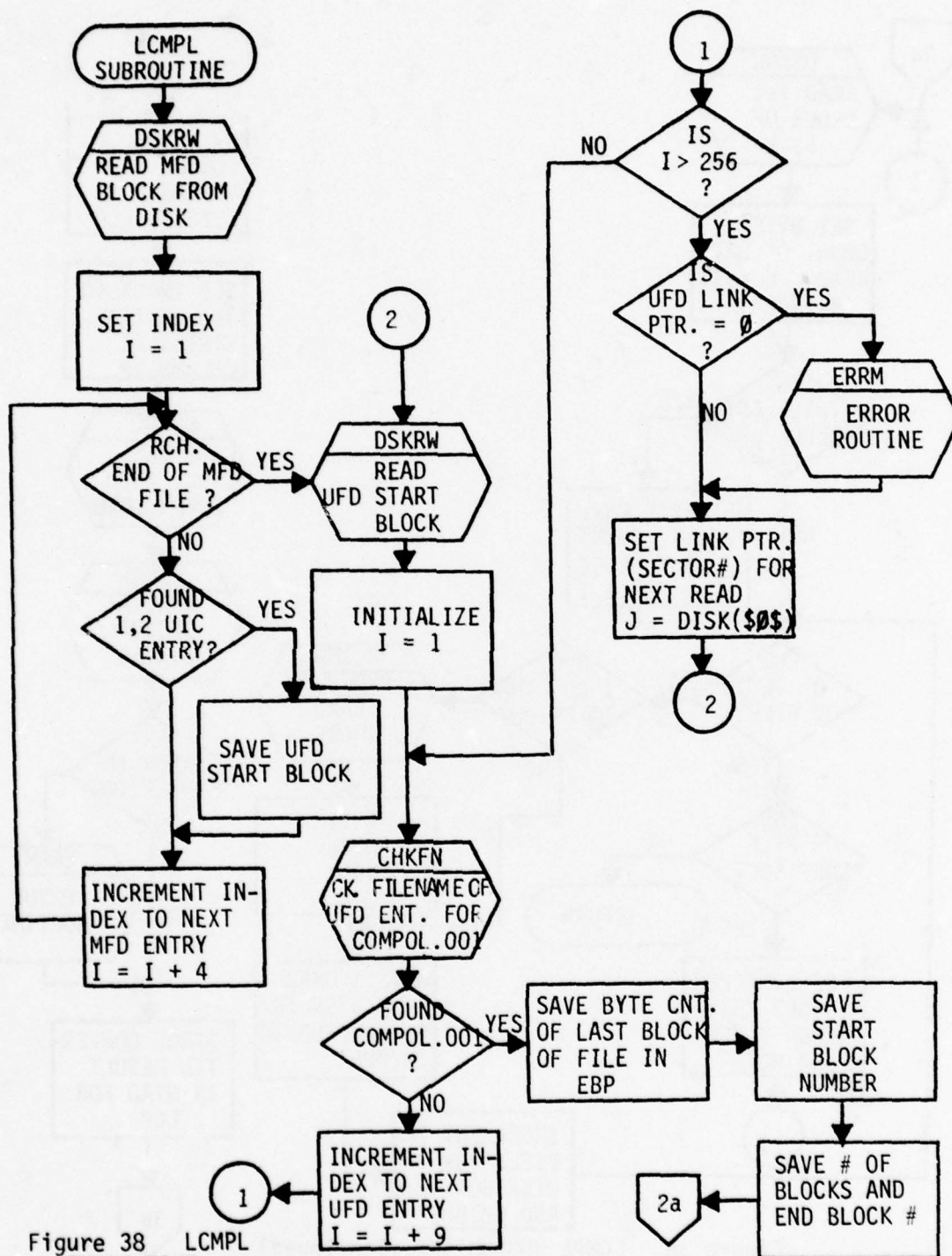


Figure 38 LCMPL
SUBROUTINE

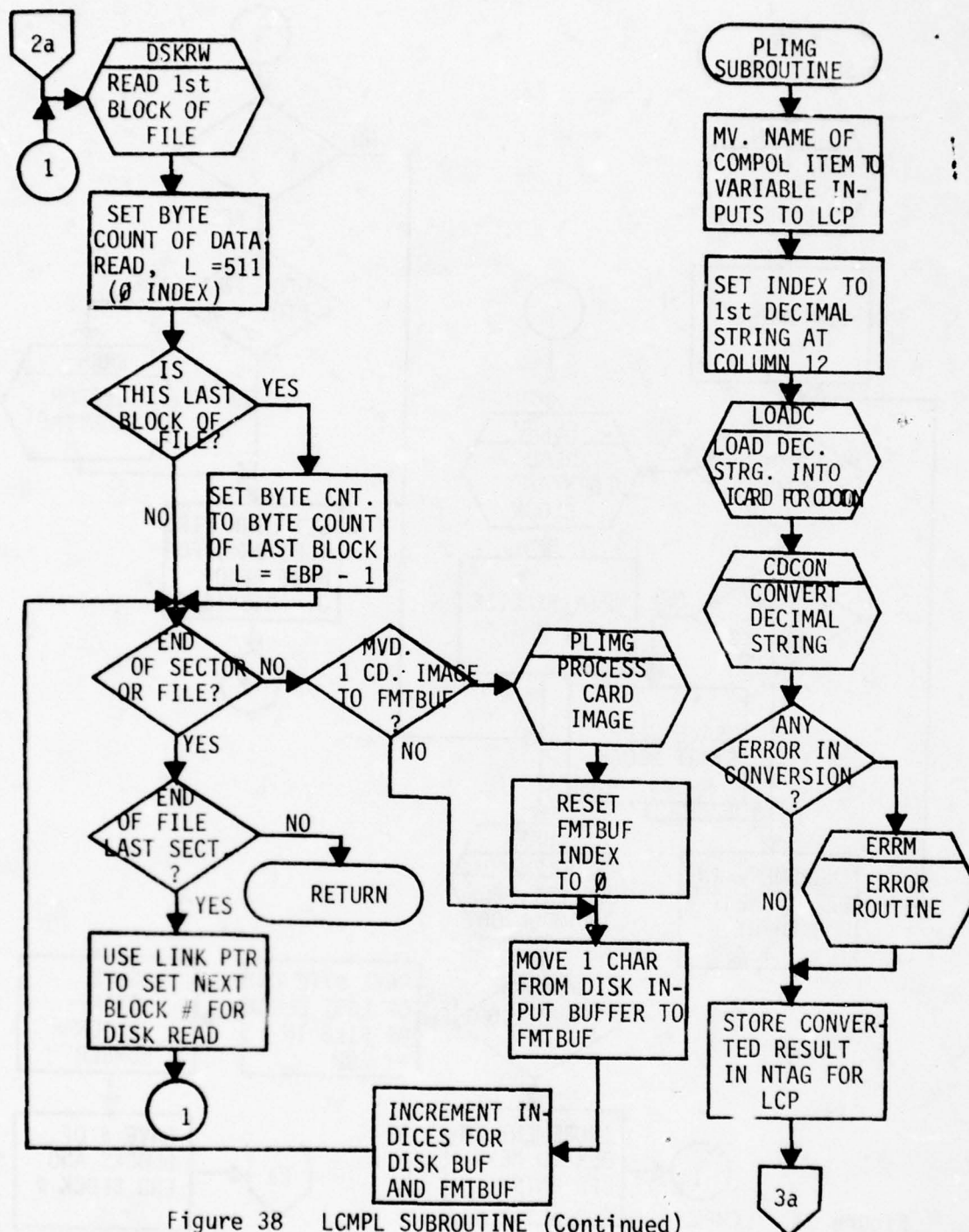


Figure 38 LCPL SUBROUTINE (Continued)

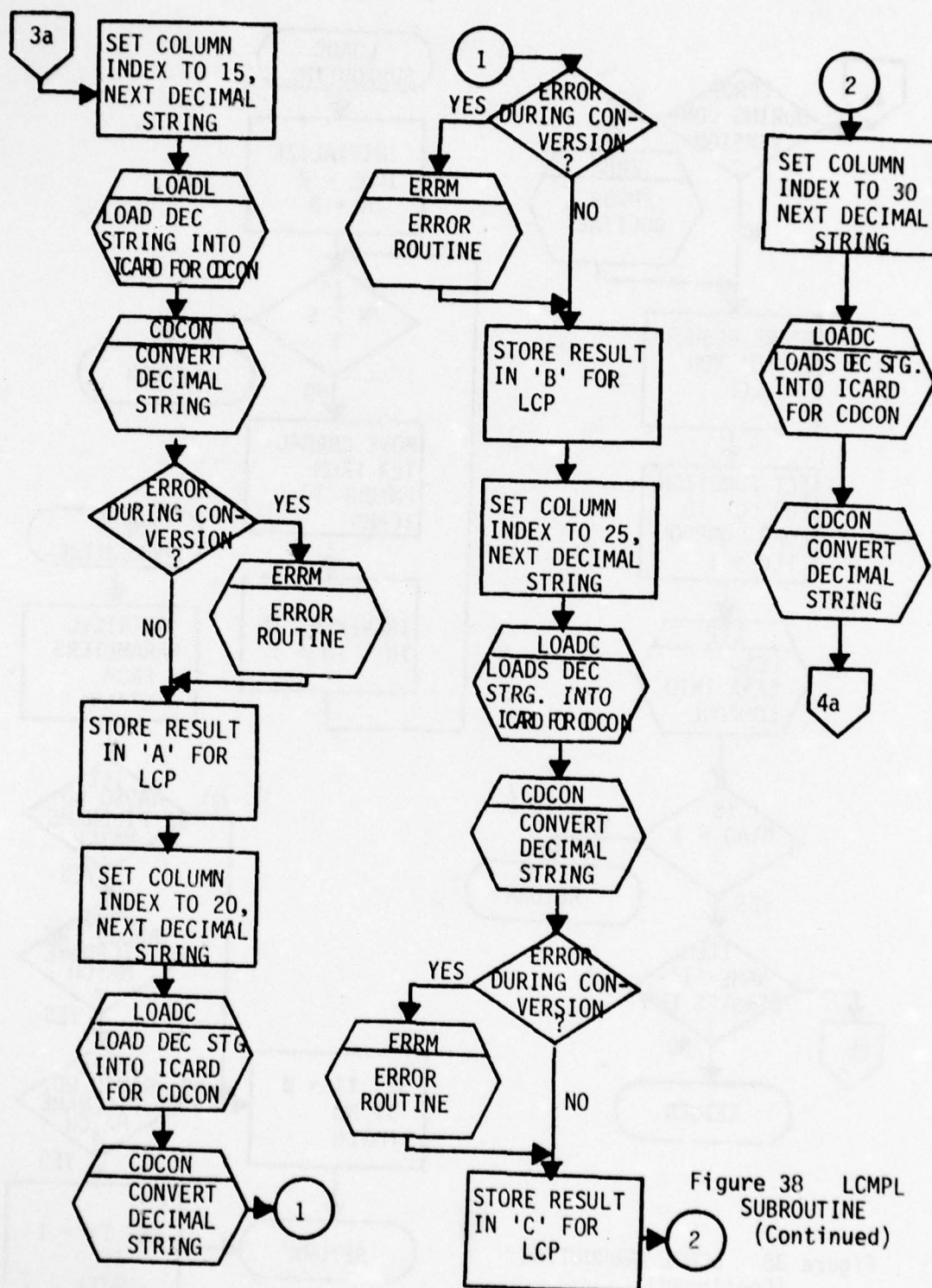


Figure 38 LCMPL
SUBROUTINE
(Continued)

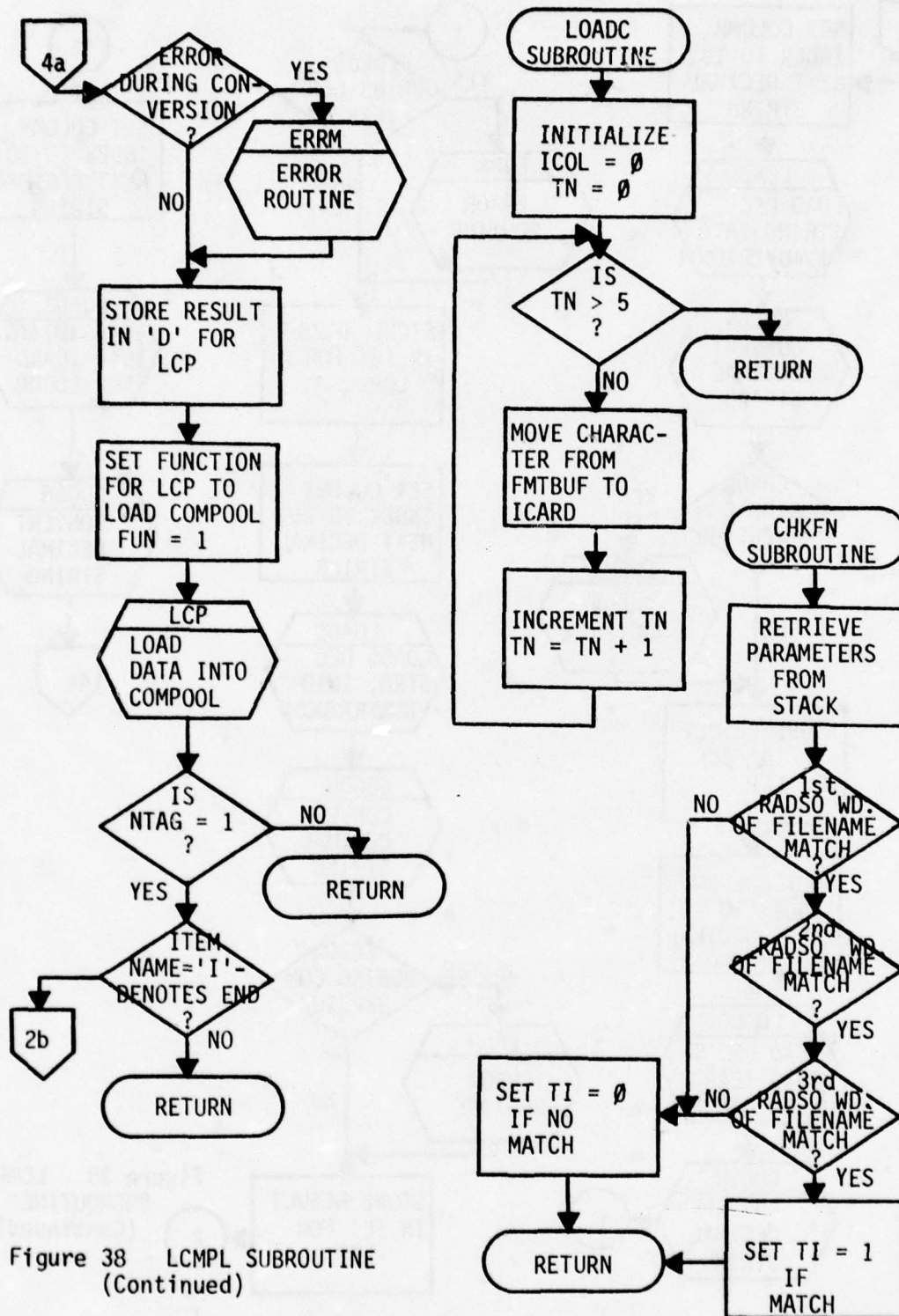


Figure 38 LCMP SUBROUTINE
(Continued)

RED-BLACK MULTIPROCESSING

6.0 RED-BLACK MULTIPROCESSING

6.1 Introduction. This section presents a promising solution to the Secure Data Base design problem. The solution, called a RED-BLACK Multiprocessing System, is demonstrably secure, conceptually simple, and quite easy to implement. Security is provided mainly by complete physical separation of data processing functions. All processing of classified data is done on one processor called the Red Processor, while all processing of unclassified data is done on another processor called the Black Processor. There is no sharing of main memory between the two processors, and communications between the Red and Black Systems are highly constrained to prohibit any classified data leakage.

Some terminals which are connected to the Black Processor System may be used for interactive processing of either classified or unclassified data. Other terminals are connected to the Black Processor System, which may be used for interactive processing of unclassified data only. (Reference Figure 39.) In the former case, requests for classified data processing are forwarded to the Red Processor by the Black, and the classified output is returned from the Red via the Black in encrypted form with decryption performed at the terminal. Thus, the Black Processor System may function in the handling of encrypted classified data, but it never has access to raw or processed classified data in plain text form.

The remainder of this section contains the following:

- Paragraph 6.2 - The threat environment is defined together with other relevant assumptions.
- Paragraph 6.3 - System design goals described.
- Paragraph 6.4 - Proposed system design description.
- Paragraph 6.5 - Proposed design security against various elements of the assumed threat environment.
- Paragraph 6.6 - Simple performance/cost evaluation.
- Paragraph 6.7 - Summary and conclusions.
- Paragraph 6.8 - References.

6.2 Threat Environment and Related Assumptions. This section summarizes the threat environment and related assumptions necessary for the System Security Evaluation discussed in Paragraph 6.4. The threat environment description consists mainly of a brief catalog of persons assumed to be potential enemy agents, together with what they are assumed to know and penetration tools at their disposal. The related assumptions pertain to persons who are assumed to not be potential enemy agents, and to the events which are assumed to be not possible. A general block diagram of the proposed RED-BLACK Multiprocessing Scheme is shown in Figure 39 to support the discussion.

6.2.1 Personnel Assumptions. Table 23 identifies all classes of persons of interest. Persons considered as potential enemy agents are referenced as (potential) agents, while those assumed to be absolutely trustworthy are referred to as good personnel. Potential agents are

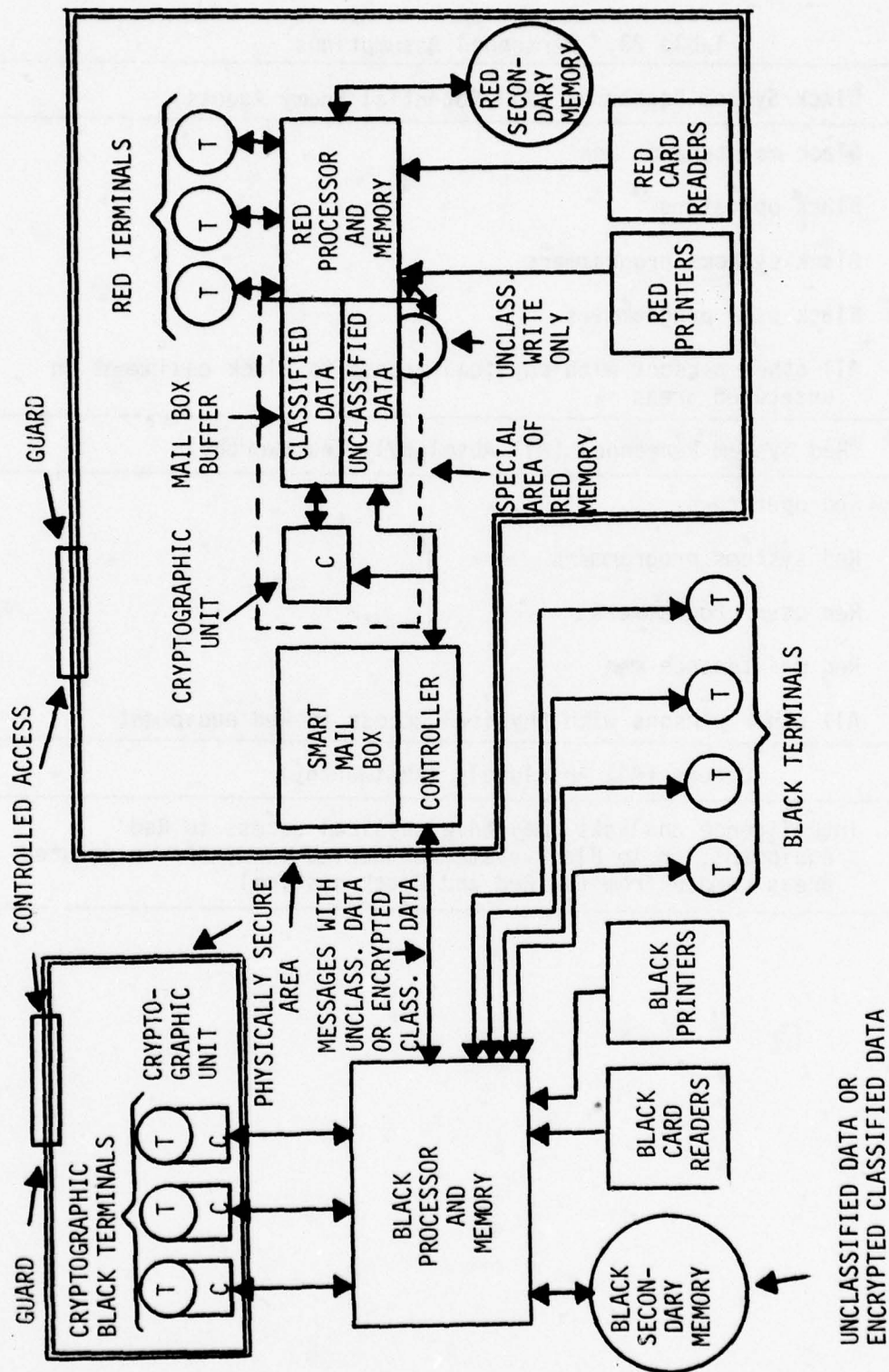


Figure 39 RED/BLACK MULTIPROCESSING SYSTEM
GENERAL BLOCK DIAGRAM

Table 23. Personnel Assumptions

Black System Personnel (All Potential Enemy Agents)	
<ul style="list-style-type: none"> ● Black maintenance men ● Black operators ● Black systems programmers ● Black user programmers ● All other persons with physical access to Black equipment in unsecured areas 	
Red System Personnel (All Absolutely Trustworthy)	
<ul style="list-style-type: none"> ● Red operators ● Red systems programmers ● Red user programmers ● Red maintenance men ● All other persons with physical access to Red equipment 	
Others (All Absolutely Trustworthy)	
<ul style="list-style-type: none"> ● Intelligence analysts (may have physical access to Red equipment, or to Black-system-connected terminals in secured areas remote from the Red and Black systems) 	

assumed to be highly intelligent, resourceful, and have access to all knowledge in possession of the enemy intelligence community; also, they are able to use all applicable enemy intelligence technology. Specifically, the potential agents are assumed to have complete knowledge of the hardware and software of both Red and Black systems. Since Black operators and systems programmers are potential agents, they are assumed to be capable of undertaking their penetration objectives under the guise of normal work activities. Because some Black terminals can be located anywhere, bad black terminal users are assumed to be able to conduct penetration efforts without concern over discovery by physical surveillance.

On the other hand, it is logical to assume that certain other classes of persons must be inherently good. In this category belong all persons with physical access of any kind to Red equipment. (Some possible exceptions to this may exist, but they will not be discussed here.)

6.2.2 Equipment Assumptions. The main equipment assumptions are:

- The cryptographic scheme used in the cryptographic units has been subjected to intense cryptanalysis, and is certifiably secure against any feasible code breaking efforts.*
- It is not feasible for any potential agent to determine a code key from physical or electronic examination of tamper-proof cryptographic Black terminals. (Harris designs and produces tamper-proof terminals for Secure Voice Communications.)
- Red system malfunctions are infrequent, and are fail-safe from a security standpoint.
- The Red system is in a physically and electronically secure area such that no potential agent can gain direct physical or electronic access to any equipment in the Red area (except for the smart mailbox, to which the potential agent has direct electronic access but not physical access).
- Black/Red System communications are solely by means of the smart mailbox as shown in Figure 39.
- There is no way for classified plain text data, processed or unprocessed to ever be placed in the smart mailbox, because of hardware controls in the Red System.

6.3 System Design Goals. It is desired that:

- The RED-BLACK Multiprocessing System be absolutely secure with respect to the threat environment identified in Paragraph 6.2.
- The system provide sufficient performance and capacity for processing all classified data and for storage of some classified data in plain text form.
- The system be easy to use;

*Such schemes are known to exist. It is assumed that one such scheme will be used.

- The system be reasonably cost-effective relative to a nonsecure system with similar performance, capacity, and ease of use.

6.4 System Design Description. Because the system design (as shown in Figure 39) is conceptually simple and involves the implementation of few new hardware or software techniques, it will not be described in full detail here. The basic idea is to:

- Enforce protection of classified data processing by complete physical isolation of the classified data processing function.
- Enforce protection of classified data transmission by using cryptographic techniques.
- Prevent classified data leakage by using a "smart mailbox" scheme to tighten control of RED-BLACK communications. This may be realized by any one of several forms of "loose" system coupling (such as disk coupling) between the Red and Black systems.

Protection of classified data processing and transmission needs little discussion because the feasibility is evident and has been already demonstrated by use. Prevention of classified data leakage is the major design feature, and must be properly implemented to ensure that leakage cannot occur. This topic is discussed in the following paragraphs.

Consider first the mailbox concept itself. At the present time it is widely used in computer systems for purposes varying from intersystem communication to interprocess communications in a multiprogrammed operating system. Because the mailbox (however implemented) is a shared resource, means must be devised to ensure that it is shared in an orderly fashion (to avoid errors, deadlock, lockout, etc.). For example, if the mailbox is a two port disk, the disk capacity must be suitably allocated for intersystem message storage. In addition, it must be absolutely secure. A typical secure RED-BLACK communications scenario might be as follows:

(Assumption: The shared disk features a smart microprocessor-based controller which independently manages the disk resource (allocates and deallocates space, etc.) and communicates with both the Red and Black Systems.)

<u>Communication Parties</u>	<u>Message</u>	<u>Action</u>
1. Black to Controller	Message for Red	---
2. Controller to Black	Ready, to receive message	Black sends message in standard format to controller. Controller stores it on disk in a location unknown to Red.
3. Controller to Red	Message from Black	---

4. Red to Controller	Ready, to receive message	Controller retrieves message for Red from an area unknown to Red, and transmits it to Red. Red stores the message in a suitable area in memory.
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6.5 Security Evaluation. The security evaluation of the proposed design is mainly concerned with the question, "Is there any way (consistent with the given assumptions) that any one of the designated potential agents can penetrate the Red system and gain access to classified plain text data?"

Given the assumptions in the system design, it seems clear that the system is secure against either accidental penetration or simple intentional penetration efforts. Note that the Red and Black systems are physically completely separate, with no communications except through the smart mailbox. If we delete the smart mailbox, then there are no communications and the complete security of the design is clearly assured. Thus, it is obvious that, if the Red system is to be penetrated at all, penetration must be via the smart mailbox. Therefore, we focus our security evaluation on that feature of the system.

Consider two basic questions which, taken together, cover all penetration possibilities. 1) Is there any way that the cryptographic key can be made to appear in the smart mailbox as a result of some Black message? 2) Is there any way that classified plain text from the Red Processor can be made to appear in the smart mailbox as a result of some Black message?

The answer to the first question is no, because the cryptographic key is not known to the Red Processor (i.e., it is not stored in the memory of the Red Processor). The cryptographic key is known only to the cryptographic units, and cannot be read by either the Red or Black Processors.

The answer to the second question is also no, provided that detail design of the Red system is suitable (i.e., error-free in design if the system is operating properly, and security fail-safe in design if there is a Red hardware malfunction). The detailed design would be quite simple, except for the requirement that each message from the Red Processor to the Black must contain some plain text information (such as information on intended recipients for the data from Red, or the destination address of the data from Red).

Given the above requirements, it is necessary to ensure that classified data can never be made to appear in the plain text portion of a Red-to-Black message as a result of any possible Black to Red message. This assurance must be provided by the Red Processor hardware and/or software. One possible scheme is to store all classified data for transfer into a fixed Red memory buffer area for transfer to the smart mailbox, and

alter the Red system hardware in such a way that any data transferred to the disk from this area is automatically encrypted by hardware (i.e., provide an encrypted-read-only Red memory buffer area). To complete this scheme, it must also be assured that the Red memory area serving as buffer area for plain text to the smart mailbox can never contain classified data. This can be done by using a data tag scheme in the Red Processor, such that all data is tagged to show whether it is classified or not (this is a special case of what is sometimes called "capability-based addressing"). The Red buffer area for transmitted plain text would then be unclassified write-only, a discipline enforced by hardware protect.

6.6 Performance/Cost Evaluation. Questions addressed in this section are:

- Would the proposed RED-BLACK scheme provide adequate performance and capacity for its intended applications?
- Would the cost be reasonable when compared with the costs of nonsecured systems of equivalent performance and capability?

The answer to the first question is difficult to provide in an absolute sense, since it is not known what the total performance and capacity requirements are for the target secure system. However, the proposed scheme is not restrictive in this regard, because a Red system of any desired performance and capacity (processor speed, memory size, secondary storage size, etc.) may be used.

The main total system performance obstructions are in the following areas:

<u>System Component</u>	<u>Area of Concern</u>
● Red Processor	Unclassified-write-only feature
● Cryptographic Unit	Encrypted-read-only feature
● Smart Mailbox	Mailbox size, speed of message transfer

Considering the obstructions in order of least concern first, we consider the Red Processor unclassified-write-only feature (used in the Red buffer for transfer to smart mailbox). Each piece of Red data to be written in this area must be associated with a tag indicating whether it is classified or not. The Red Processor unclassified-write-only feature prevents the writing to the buffer of any data which is classified by tag checking. The tag checking must be done with every piece of data, but it can be accomplished rapidly using standard hardware methods and should have little effect on the overall system performance.

The performance of the cryptographic unit used with the encrypted-read-only is likely to be more of a problem. For example, Motorola now markets an LSI-based cryptographic unit for the NBS standard encryption scheme which requires 160 microseconds for encryption/decryption of 8 bytes of data, or 20 microseconds for encryption/decryption of each byte of data.

For a similar device, Stanford (optimistically) estimates that the encryption job can be done in 1 microsecond by an LSI chip, while NBS is estimating 40 microseconds (or 5 microseconds per byte). Thus, it appears that the additional time required to encrypt/decrypt large data files with a suitable secure scheme may be fairly significant (for the near future anyhow).

The performance of the smart mailbox is the most critical potential obstruction in the proposed scheme. Limiting the performance of the smart mailbox are the processor-to-mailbox dialogs that must take place, and the technology used to implement the smart mailbox.

The dialogs constitute an overhead which is most troublesome if typical messages are short. However, it should be understood that in any multiprocessor system, any workable communication scheme using some form of shared storage must inevitably be associated with some overhead due to the need for management of the shared resource. For example, if the mailbox is built from shared main memory, devices such as Dijkstra's P and V operators and semaphores are needed to ensure that one processor is not writing into a shared area at the same time another processor is reading from it. Thus, some smart mailbox management overhead is inevitable regardless of the particular mailbox storage technology used.

Disk technology is a promising candidate for mailbox storage because it is quite fast and yet provides a large mailbox (for big messages or large numbers of messages) at a fairly low cost. Two ports may be provided for the disk to allow concurrent message transfers, and this potentially doubles performance over a single port scheme. For example, the Black Processor can be writing one message in the disk at the same time the Red Processor is reading a different message from it. However, if a disk mailbox is too slow, it is possible to significantly improve smart mailbox performance by building it with another storage technology, such as drum or a separate segment of main memory.

If disk technology is used, data transfer rates may be high (800K bytes per second) and performance will be fairly good (relative to a RAM mailbox) for longer messages. However, for short messages the large access average access time of a disk (typically around 25 ms) relative to core (typically about 1 μ s) may make the device up to 25,000 times slower than an equivalent RAM mailbox. Whether or not this fact would make the disk mailbox unacceptable for the human user (response times in seconds) has not been determined.

The RED-BLACK multiprocessor cost evaluation may be considered as follows:

- Consider the cost of multiprocessor system versus uniprocessor systems, generally.
- Consider the additional cost of special security features. The features are briefly discussed in the following paragraphs.

6.6.1 Multiprocessor Versus Uniprocessor System Cost. Whether or not a multiprocessor system is cost-effective relative to a uniprocessor system of equivalent performance is a subject which has been debated in the computer industry for many years. The question has not been fully resolved, and it may never be. Suffice it to say here that dual processor systems are now quite common, having survived the cost/effectiveness test of the marketplace. Therefore, we may conclude that, while all possible multiprocessing systems may not be cost-effective, some certainly are. We assume that the RED-BLACK Multiprocessor scheme proposed here can be suitably designed so as to fall in the latter class.

6.6.2 Special Security Features Cost. The special security features proposed are:

- Use of cryptographic units for Red processor encrypted-read-only.
- Use of data tags for Red processor unclassified-write-only.
- Use of a smart mailbox.

Cryptographic units can now be built with LSI technologies at low cost. For the NBS standard encryption scheme, Motorola now has a small board selling for about \$500, and expects to offer a hybrid device soon for about \$150. Fairchild offers an NBS standard unit built from four chips, with the price of the four chips currently about \$30. Thus, we conclude that the cost of a cryptographic unit will not be very high, mainly because it can be built using low cost LSI technology.

The unclassified-write-only feature for the Red Processor is a special case of capability based addressing, a technique which is considered by some to be an attractive partial solution to the secure computer system design problem. To implement full-fledged capability-based addressing requires a new Red Processor architecture, and this can be extremely expensive to implement (assuming the Red Processor does not already possess the feature). For an interim solution, this feature would probably be best provided by a special box which intercepts all Red Processor/Memory transactions and imposes the desired control. Such a box could probably be designed and built on a one-time basis for a few thousand dollars.

The major hardware cost item for the proposed design would be the smart mailbox. At present, it could best be built using microprocessor-based disk controller (assuming the disk mailbox offers sufficient performance). A suitable disk (14 megabyte capacity) costs about \$10,000 and the controller could be designed and built by Harris ESD for about \$30,000. However, it is possible that a suitable smart disk control unit already exists on the market which could be modified for the job (there is a general trend toward the use of smart disk controllers). If so, substantial savings might result by purchasing and modifying such a device.

6.7 Summary and Conclusions. A RED-BLACK Multiprocessing scheme has been described as a promising solution to the Secure Data Base System design problem. The scheme is conceptually simple, demonstrably secure,

offers good performance, and can be implemented from conventional computer system components with relatively small additional cost for the security features.

A typical system using this scheme is basically a loosely-coupled two processor multiprocessing system which employs cryptography for classified data transmission and a smart mailbox for communications between the two processors. The smart mailbox can be constructed using disk storage and a microprocessor-based controller; but for higher performance, it can be built using a drum or RAM for message storage. Cryptography and the smart mailbox (with associated Red Processor memory address modifications) are the keys to the system's security. Security is easily demonstrated, mainly because of the conceptual simplicity of the scheme employed. The basic system cost should be only slightly higher than the cost of a similar multiprocessing system without the additional security features, because the latter can be provided for an estimated \$40,000 or less.

Overall, it is concluded that the proposed design approach is a promising one, because it is demonstrably secure while providing potentially high performance, capacity and cost effectiveness.

The first part of the report is a summary of the work done in the last year. This is followed by a detailed description of the work done in the last year. The report then discusses the results of the work done in the last year. The report concludes with a summary of the work done in the last year.

SECTION 7.0

DATA BASE GUARD APPROACH

7.0 DATA BASE GUARD APPROACH

This section examines the feasibility of a multiported disc controller that acts as a guard between the data base and one of several computers. Control is accomplished by allowing access to only the secret computer. Attempts to access a Top Secret record will be disallowed by guard checks of the record classification.

7.1 A Protection Scheme. When a data base resides in a disk storage system and the users are separate computer systems it is possible to protect sensitive data from unauthorized access by building the protection mechanization into the multiported disk controller. Consider the system architecture shown in Figure 40 and the following protection mechanism. A multiported disk system is connected to several user computer systems with each storage system interface assigned an access privilege level. Every sector on the disk contains a security access word as part of the sector format. When a user computer requests an access to a disk sector the controller reads the access control portion of the disk format first and only honors the request if the sector has a security level less than or equal to the access privilege level assigned to the users I/O interface. This scheme provides a multiported storage system with hardware protection of sensitive data. Several questions which must be answered in order to evaluate the data protection scheme are:

- Does this scheme adequately protect the data records in various file structures?
- What constraints does the protect scheme place on the selection of file structure or on the logical records to physical-storage mapping?
- How can write protection be implemented; i.e., how does the data base change?
- How can space allocation be handled?
- How is the access speed of the system affected by the protection scheme?

The answers to these questions must be found by examining some of the mechanics of file structures and systems.

7.2 The Data Base: Files and Records. The data stored in a data base is contained in logical entities called records and is the smallest amount of information that can be directly accessed. The records are grouped together into larger structures called files. Physical storage of a file is usually made up of a number of blocks which are the smallest physical access that a file system makes to the storage device. The logical records of a file are mapped onto the blocks. For disk storage systems this is usually an integer number of disk sectors. The blocks of a file are identified by the "file access mechanism." There are hundreds of file access mechanisms or structures but in the interest of brevity only two of the most common will be examined. One is called block linking and the other is record indexing. Figure 41 illustrates both methods. Linked files are often used for files which are sequentially accessed. The access for one

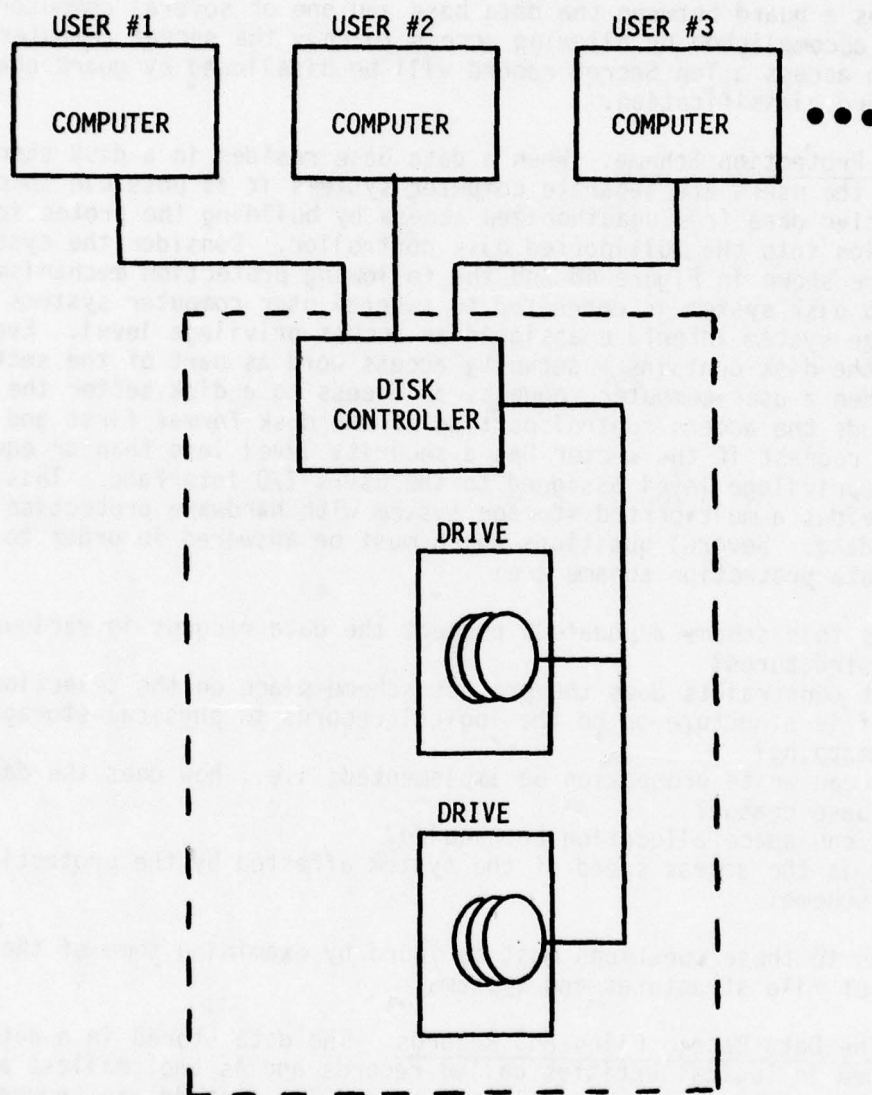
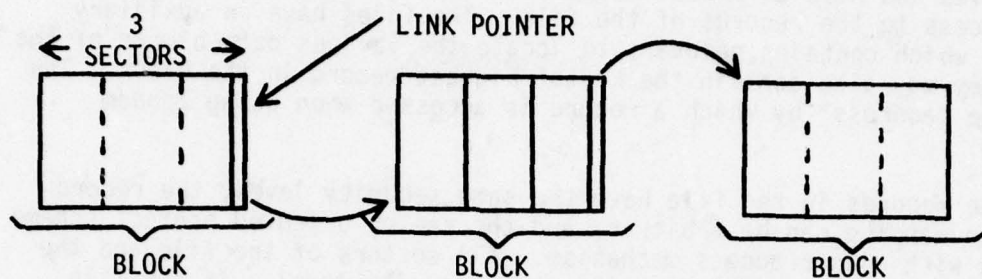
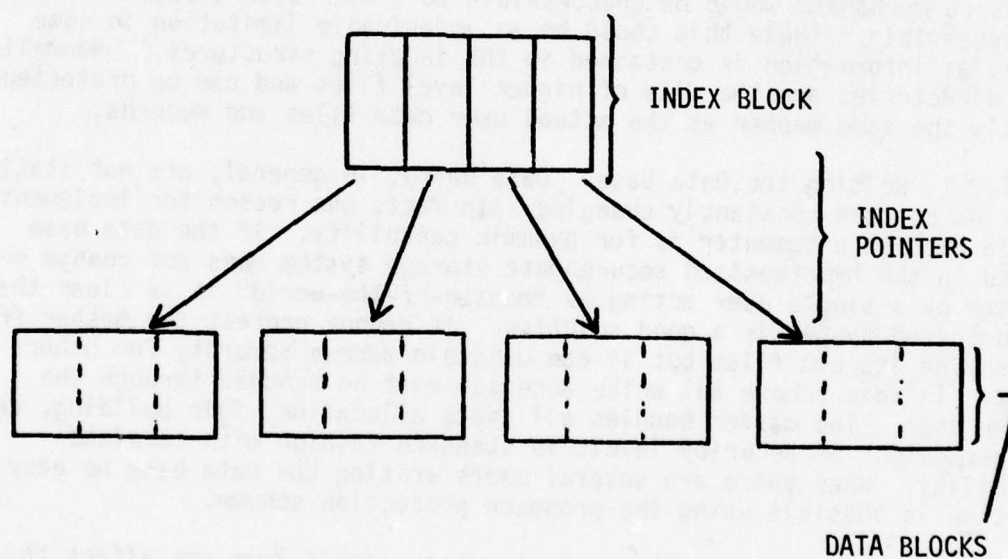


Figure 40 THE SYSTEM



FILE CONSISTS OF 3 BLOCK OF 3 SECTORS/BLOCK



FILE CONSISTS OF 4 DATA BLOCKS OF 3 SECTOR/BLOCK
AND 1 INDEX BLOCK CONTAINING ONLY 4 POINTERS

Figure 41

block of data gets the pointer for the next. Thus, there is very little overhead in either time or storage. Indexed files are used for random access files and have an access mechanism which allows more efficient random access to the records of the file. The files have an auxiliary structure which contains pointers to locate the various data blocks of the file. They may also contain the key of highest record in the block. The key is the "address" by which a record is accessed when using random accessing.

If the records in the file have the same security level, the record-to-storage mapping can be arbitrary and the sector oriented protect scheme will work with either access mechanism. All sectors of the file and the index structure if used can have the same security level. If the file contains records of different security classifications a linked structure is impossible since a lower classified user would not be able to follow the links. If the file is of the index type the only requirement is to ensure that two records of different security classifications do not share storage in the same sector. In general, it would also be necessary that the index blocks have the security level of the lowest record in the file or the accessing mechanism would be inaccessible to a user even though the data was accessible. (Note this could be an undesirable limitation in some cases, as information is contained in the indexing structures.) Normally file directories are the data of higher level files and can be protected in exactly the same manner as the actual user data files and records.

7.2.1 Writing the Data Base. Data bases, in general, are not static entities but are constantly changing. In fact, one reason for implementing a data base on a computer is for dynamic capability. If the data base stored in the hypothesized secure data storage system does not change or is written by a single user acting as "master-of-the-world" it is clear that the proposed system is a good solution. It cannot protect the master from destroying its own files but it can maintain access security for other users. In this scheme all write accesses must be handled through the master user. The master handles all space allocation, file building, and the assignment of security levels in standard fashion with complete visibility. When there are several users writing the data base no easy solution is possible using the proposed protection scheme.

7.2.2 Access Speed. The protect scheme itself does not affect the access speed of the proposed system architecture. Rather, it is the architecture which suffers access speed limitations. A sequential access controller can be used when disk access rates are slow, but when the number of users and the access rate increase, the architecture will suffer from a significant amount of disk arm movement and rotational latency. In this application, a sophisticated controller can improve system performance by using sector queuing and overlapping seeks with data transfer operations. This sophistication makes the controller look more like a complete processor based file system, than a simple controller.

7.2.3 Design. The following design is an example of a multiported disk controller which provides sector data protection. The design is a controller for the Diablo series 400 disc drives. User interfaces are intended to connect to PDP-11 users. The goal was to provide a basic design which could handle eight disk drives or a maximum storage of 170 million words (using the biggest Diablo 400 series drive) and service at least three users with easy expansion. Automatic handling of multiple seek operations complicates the controller but makes the design more realistic for median loading of the storage system.

Figure 42 shows the disk storage system design consisting of from one to eight Diablo disk drivers. A control bus runs from the controller to each drive in a wired or bus fashion. A bidirectional data cable and a clock cable run individually from each drive to the controller. Control and status information is passed from the controller to the drives via the common control bus while the data and clock signals are handled on separate cables. The PDP-11 computers are connected to the disk controller via the Controller Interface Units (CIU's) and the CIU Bus. Figure 42 shows the CIU Bus connecting one CIU to the next, however, the design does not preclude a multilegged star type configuration.

Figure 43 shows the sector format which will be supported by the disk controller. The format contains an error coded security tag as the first part of the sector. The control will read the tag and pass the data portion of the sector to the requesting user if the user has a security level greater than or equal to the tag. The format is compatible with Diablo drive requirements.

7.2.4 The CIU Bus. The CIU bus is a simple communication bus between the disk controller and the individual CIU. Data transfers via the bus are 16 bits wide with a maximum transfer speed of about 700K words per second. Bus mastership is always held by the controllers. The bidirectional bus data lines (reference Figure 44) are time shared for data and address. The address is shown in the select format.

7.3 The CIU Software Interface. Figure 45 shows the software interface to the protected storage system. The interface consists of 4 registers in the device space of the Unibus. The first register specifies the drive and cylinder number. The second register specifies the track and sector number for the access and the length of the transfer in integer number of sectors. (Each sector contains 256 words of data.) The complete Unibus Transfer address is specified in the remainder of the second register and all of the third. The fourth register is the status and control register with a format very similar to the standard DEC interface.

The controller will support read operations for all CIU's. A read will only get the data portion of a disk sector. The write function is limited to special users as specified by a ROM table in the controller and will write the access level word and 256 words of data. The access word is appended to the front of the data buffer to be written, i.e., for an N sector write the buffer would have to be NX257 words.

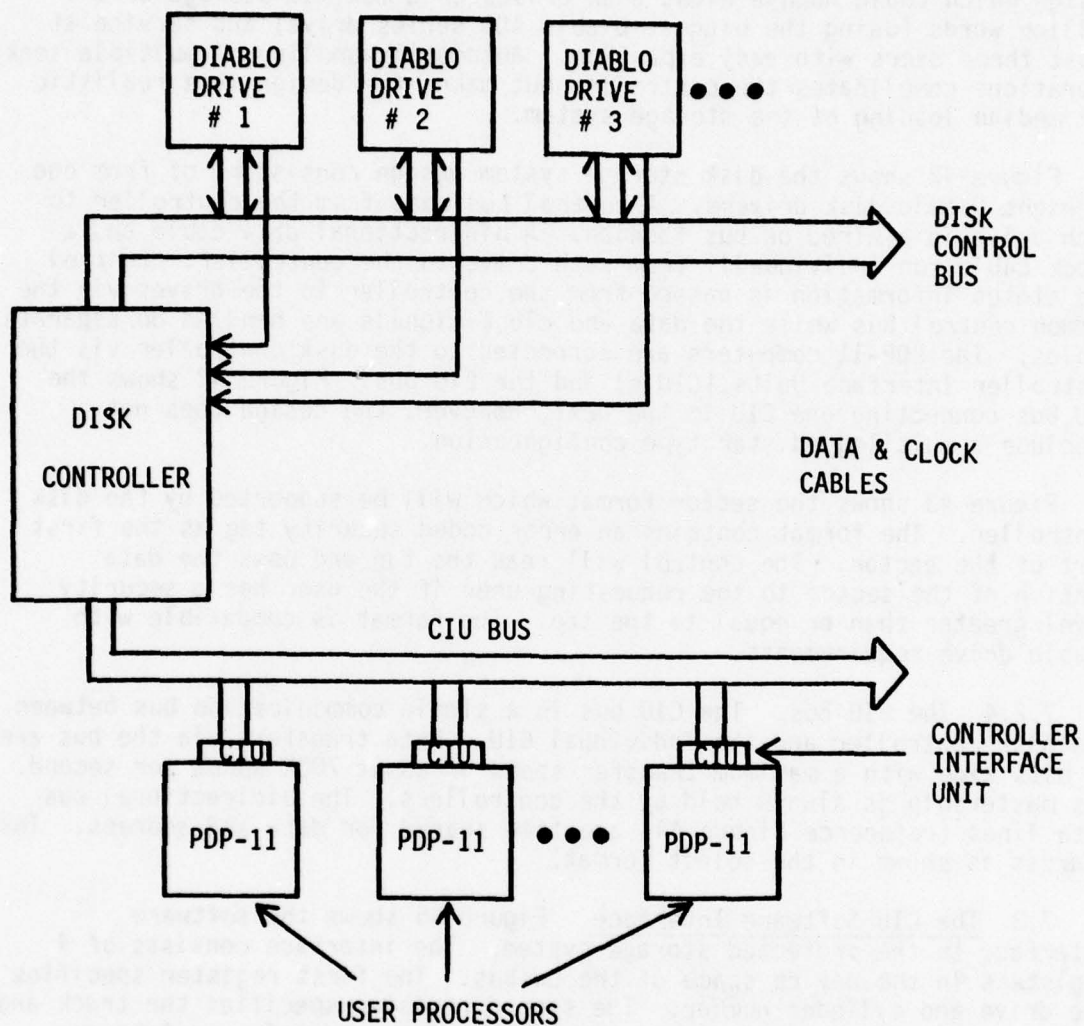
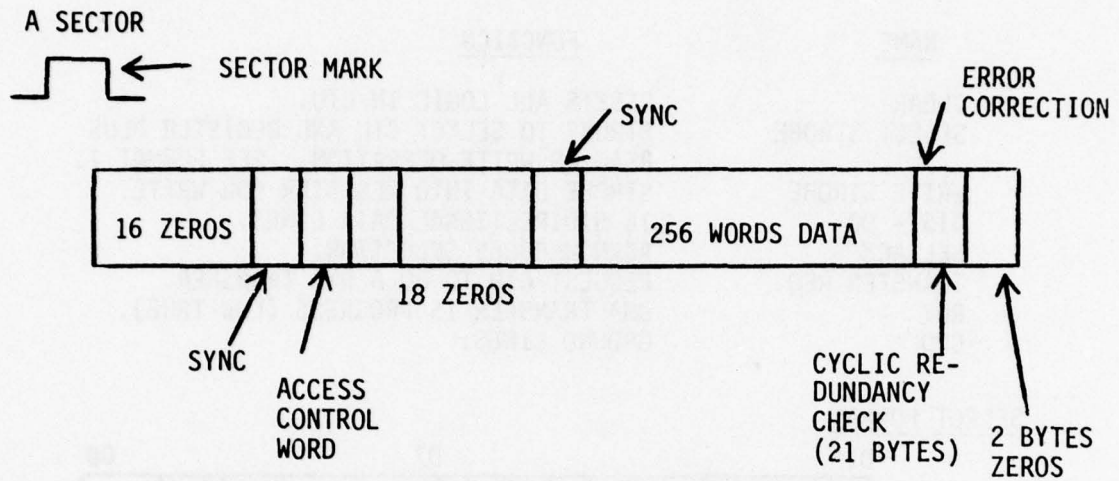


Figure 42

SECTOR FORMAT



SYNCS: FRAME SYNCHRONIZERS (8 DATA BITS LONG)
ACCESS CONTROL WORD IS ERROR DETECTION/ENCODE

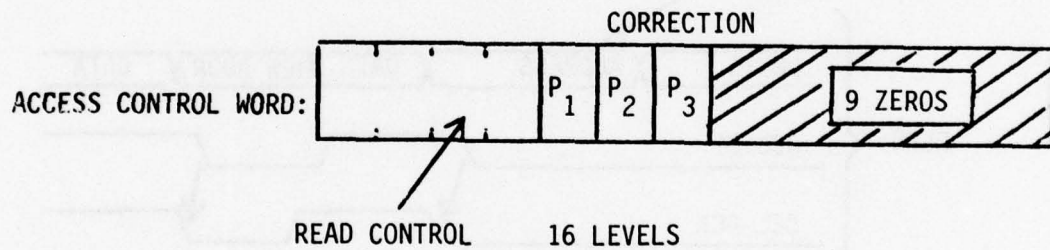
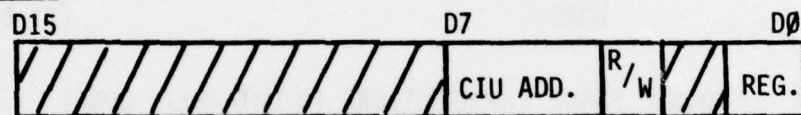


Figure 43 SECTOR FORMAT

THE CIU BUS

<u>NAME</u>	<u>FUNCTION</u>
CLEAR	RESETS ALL LOGIC IN CIU.
SELECT STROBE	STROBE TO SELECT CIU AND REGISTER PLUS READ OR WRITE OPERATION. SEE FORMAT 1.
WRITE STROBE	STROBE DATA INTO REGISTER FOR WRITE.
D15 - D0	16 BIDIRECTIONAL DATA LINES.
SEL ACK	ACKNOWLEDGES SELECTION.
TRANSFER REQ.	REQUEST CIU TO DO A DMA TRANSFER.
RDY	DMA TRANSFER IS PROGRESS (LOW TRUE).
GND	GROUND LINES.

SELECT FORMAT



TIMING

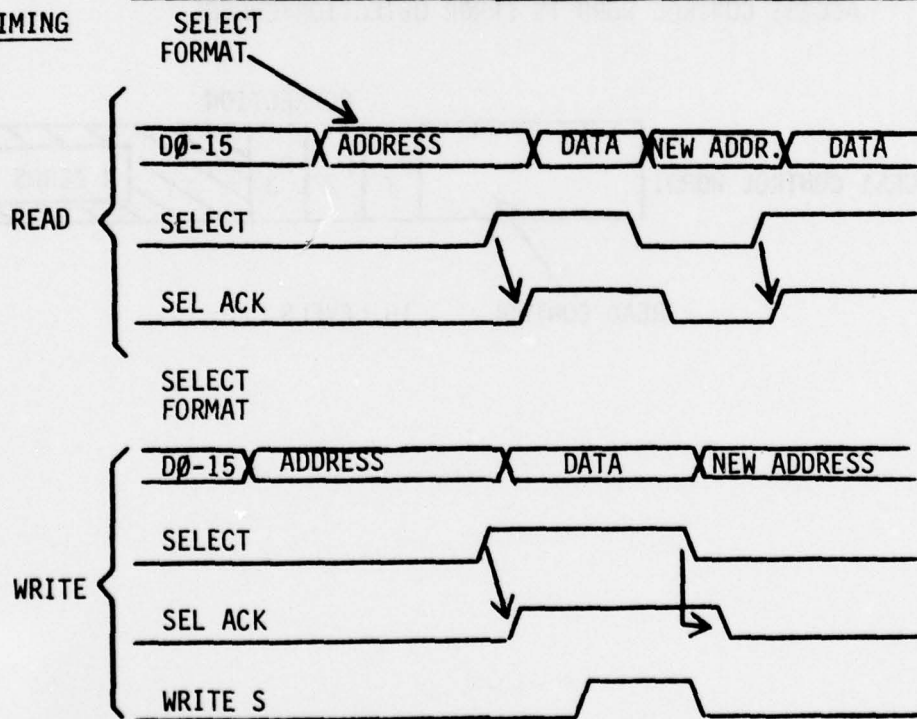


Figure 44 THE CIU BUS

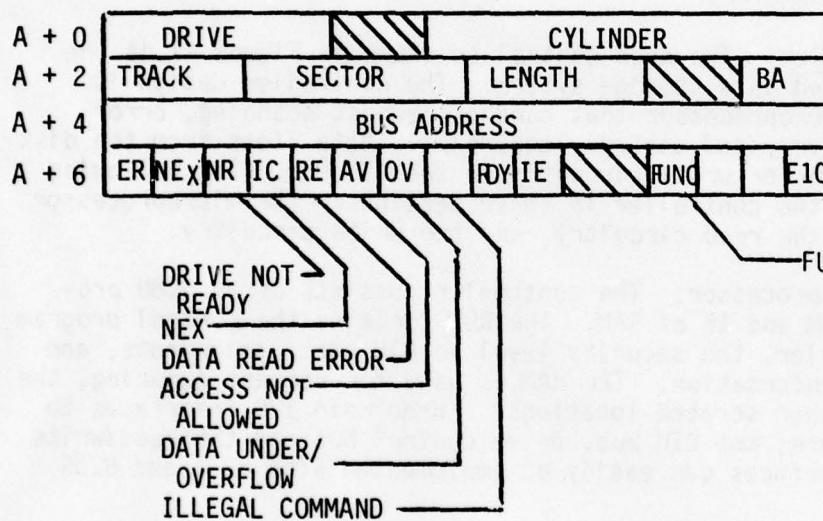


Figure 45 USER SOFTWARE INTERFACE

7.4 The CIU Hardware. The CIU is the hardware interface between the disk storage system and the user's PDP-11 processor. Figure 46 shows the basic block diagram of the CIU. The Unibus side of the CIU contains the basic address decoding and slave response logic to support four Unibus address locations as the I/O control registers. In addition, it contains logic to perform 16-bit DMA transfers. Because the registers of the CIU are accessed from two sources, the interface operates in a special manner. Prior to issuing a Go command the registers can not be accessed by the controller over the CIU bus, but can be read or written by the PDP-11 processor. Once the Go command has been issued the registers are released for access over the CIU bus and can not be meaningfully accessed from the Unibus. An access from the Unibus will always get zero. When the service request is finished the register will become accessible to the Unibus again.

DMA transfers between buses are accomplished when the controller has bus control of the interface. The address for the DMA transfer is contained in the address register of the CIU and is incremented by two at the completion of each transfer.

7.5 The Controller. The disk controller shown in Figure 47 is the heart of the protected data storage system. The controller design is centered around a microprocessor that handles request scanning, error checking, error recovery and control sequencing. Data flows from the disk drive through the read or write circuitry to the CIU bus. The following paragraphs describe the controller in three sections: the microprocessor and its interfaces, the read circuitry, and the write circuitry.

7.5.1 The Microprocessor. The controller consists of an 8080 processor with 4K of ROM and 1K of RAM. The ROM contains the control program for the disk controller, the security level to CIU port assignments, and some configuration information. The RAM is used for request queueing, the program stack and other scratch locations. Three main I/O interfaces to the microprocessor are; the CIU bus, drive control bus and the read/write circuitry. The interfaces can easily be implemented with 8212 and 8255 chips.

The drive control bus is the path the controller uses to command the drivers and is oriented for 8-bit microprocessors. Figures 48, 49 and 50 contain specifications of the bus as per Diablo documentation.

The microprocessor's function is to gather access requests from the users, send the appropriate commands to the drivers and the read/write circuitry, and monitor status and possible error conditions. Figure 51 is a simplified flow chart of the firmware that the microprocessor would execute. The complete firmware would include fault diagnostics and error recovery code along with initialization and setup operations. Sizing of the code shows that all the tasks can be accomplished in less than 3000 bytes of program and tables. The small amount of code makes verification of it easier and since it is in ROM it is safe from tampering.

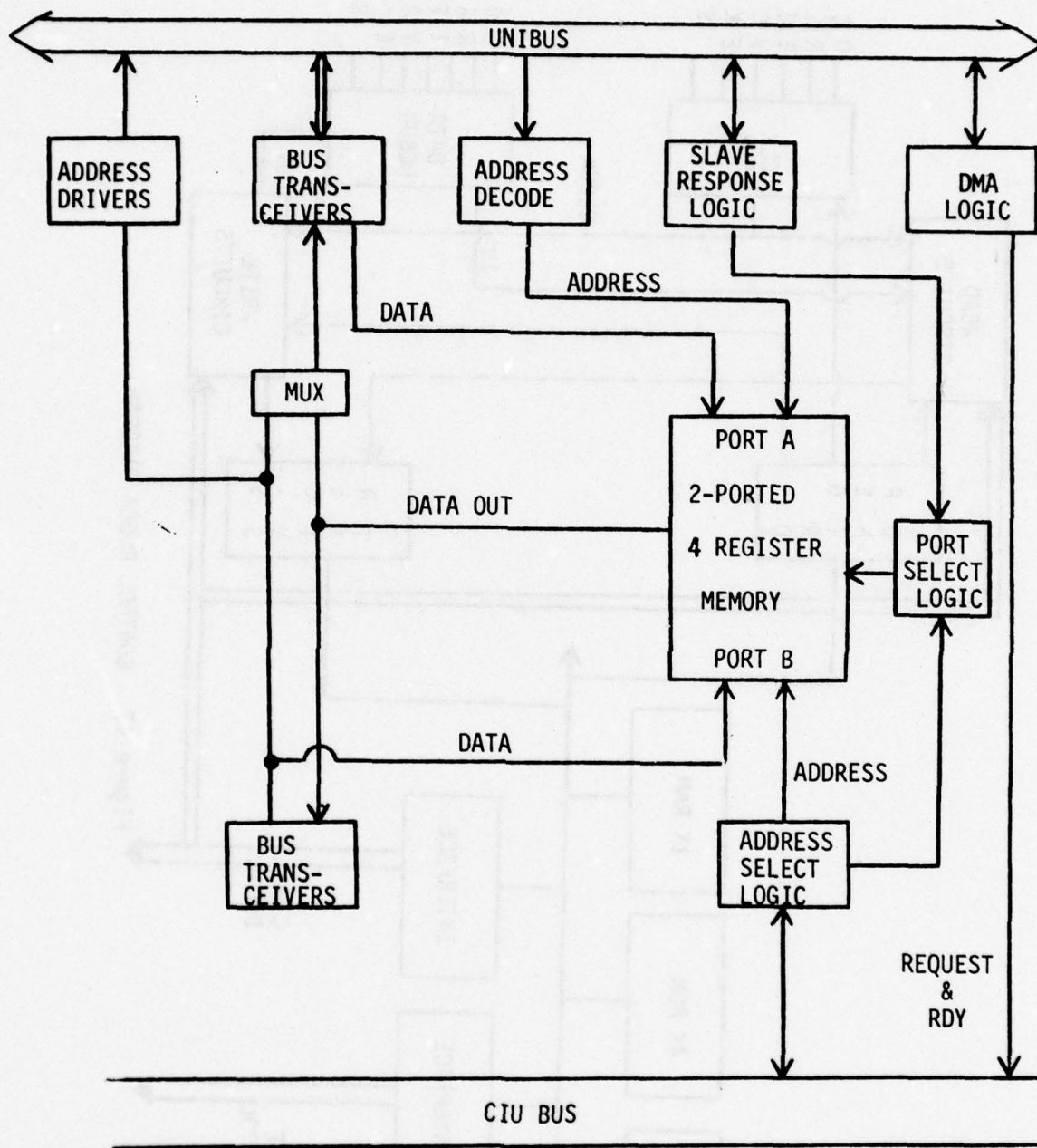


Figure 46 CIU HARDWARE

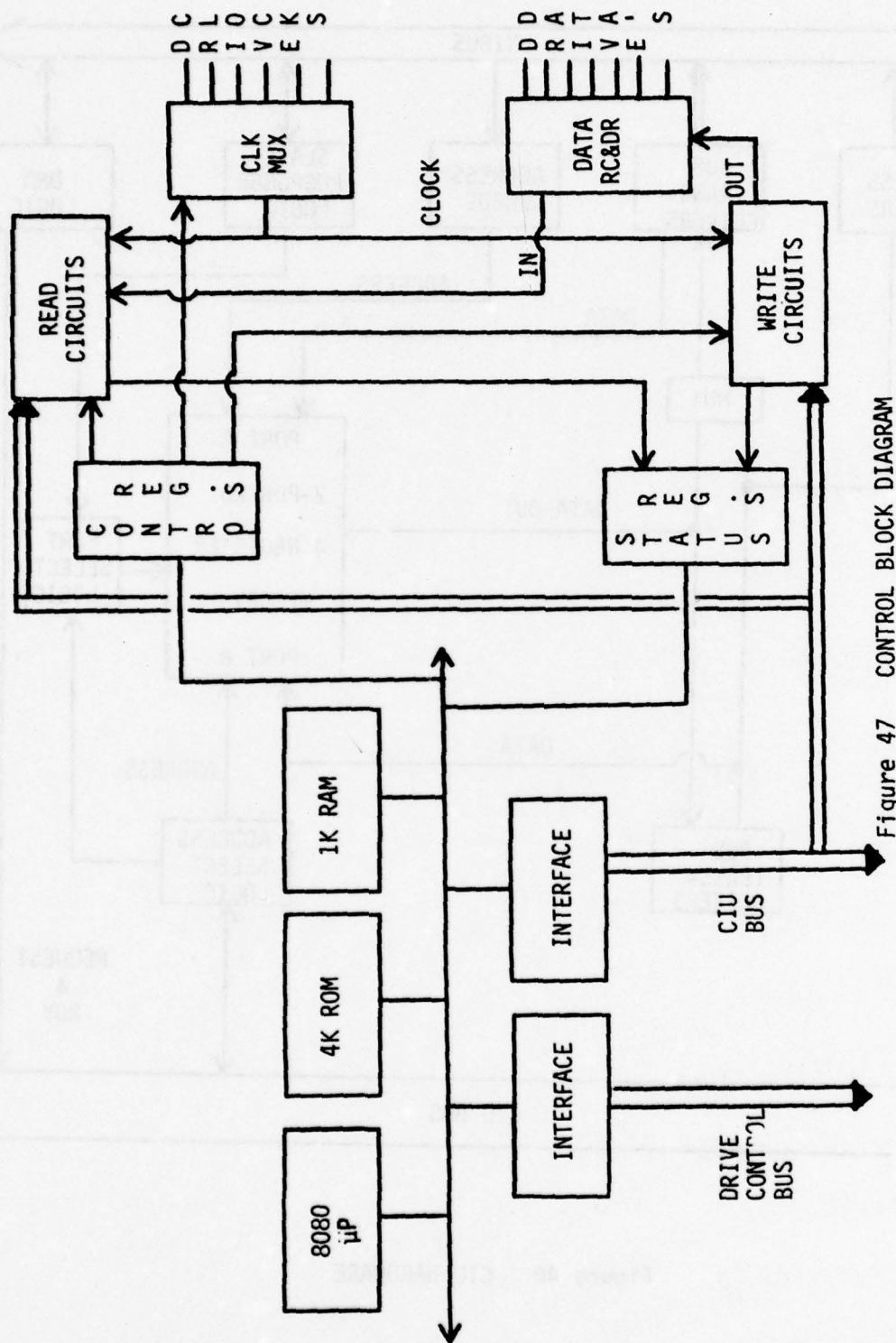


Figure 47 CONTROL BLOCK DIAGRAM

CONNECTOR 'A' PIN ASSIGNMENTS

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
1	GND 1	Ground.
2	Spare 1	Not used.
3-10	Control Bus (Bits 0-7)	Control Bus transfers disk unit select codes, command codes, and information bytes from controller to disk drive. Transfers status, mode, and sector counter bytes from disk drive to controller.
11	-SYSTEM CLEAR	When low, this signal deselects disk drive and clears input and output ports.
12	+SELECT STROBE	Strobes disk unit select code from control bus into drive.
13	+INPUT STROBE A	Strobes restore, cylinder and head commands into the input port. Also, sets "Input Full" and "Busy" status in mode byte.
14	+INPUT STROBE B	Strobes all commands (other than restore, cylinder and head) into the input port. Also, sets "Input Full" status in mode byte.
15	+OUTPUT ENABLE	Gates the contents of the disk drive output port onto the control bus, to be read by the controller. Also, resets "Output Full" mode bit.
16	+MODE ENABLE	When high, this signal gates the mode byte of the selected unit onto the control bus.
17	+SECTOR ENABLE	When high, this signal gates the contents of the sector counter for the selected unit onto the control bus.
18	+ATTENTION PULSE	A 500 ns pulse transmitted anytime an important change of status occurs in any unit.
19	+SECTOR PULSE	Indicates the beginning of each sector for timing the start of read or write. Also represents period of stable sector count.

Figure 48. Drive Control Bus Specifications (1 of 2)

CONNECTOR 'A' PIN ASSIGNMENTS (Continued)

<u>PIN</u>	<u>SIGNAL</u>	<u>DESCRIPTION</u>
20	+WRITE GATE	Controls beginning and end of data writing. +WRITE GATE should remain high for two bit periods after last data bit intended to be written on disk.
21	+READ GATE	Controls beginning and end of data reading.
22-24	Spare 2-4	Spare pins.
25	Spare 5	Not used.
26	GND 2	Ground.

Figure 48. Drive Control Bus Specifications (2 of 2)

COMMAND FORMAT

COMMANDS	CLASS	CONTROL BUS							
		7	6	5	4	3	2	1	0
Restore		0	0	0	0	0	0	0	1
Cylinder (followed by 2 bytes)	A	0	0	0	0	0	0	1	0
Head (followed by 1 byte)		0	0	0	0	0	0	1	1
Status Request A		0	0	0	0	0	1	0	0
Status Request B		0	0	0	1	0	1	0	0
Status Request C	B	0	0	1	0	0	1	0	0
Status Request D		0	0	1	1	0	1	0	0
Reset Write Protect*		0	0	0	0	0	1	0	1
Set Write Protect*		0	0	0	1	0	1	0	1
Track Offset In +3 Δ *		0	0	1	1	0	1	1	0
Track Offset In +2 Δ *		0	0	1	0	0	1	1	0
Track Offset In + Δ *		0	0	0	1	0	1	1	0
On-Track*		0	0	0	0	0	1	1	0
Track Offset Out - Δ *		1	0	0	1	0	1	1	0
Track Offset Out -2 Δ *		1	0	1	0	0	1	1	0
Track Offset Out -3 Δ *		1	0	1	1	0	1	1	0
Diagnostic Test A*		0	0	0	0	0	1	1	1
Diagnostic Test B*		0	0	0	0	1	0	0	0
Diagnostic Test C*		0	0	0	0	1	0	0	1

* Not to be issued when drive is busy.

Δ Represents fraction of track width; typically 100 microinches.

Figure 48. Drive Control Bus Specifications (1 of 2)

ADDRESS FORMAT									
ADDRESS	CLASS	7	6	5	4	3	2	1	0
Unit Select Code	C	X	X	X	U ₁₆	U ₈	U ₄	U ₂	U ₁
Cylinder Address MS (2nd byte)		X	X	X	X	X	X	C ₅₁₂	C ₂₅₆
Cylinder Address LS (1st byte)	B	C ₁₂₈	C ₆₄	C ₃₂	C ₁₆	C ₈	C ₄	C ₂	C ₁
Head Address		X	X	X	X	H ₈	H ₄	H ₂	H ₁

NOTE: Class A commands use Input Strobe A, Class B commands use Input Strobe B, and Class C commands use Select Strobe.

Figure 48. Drive Control Bus Specifications (2 of 2)

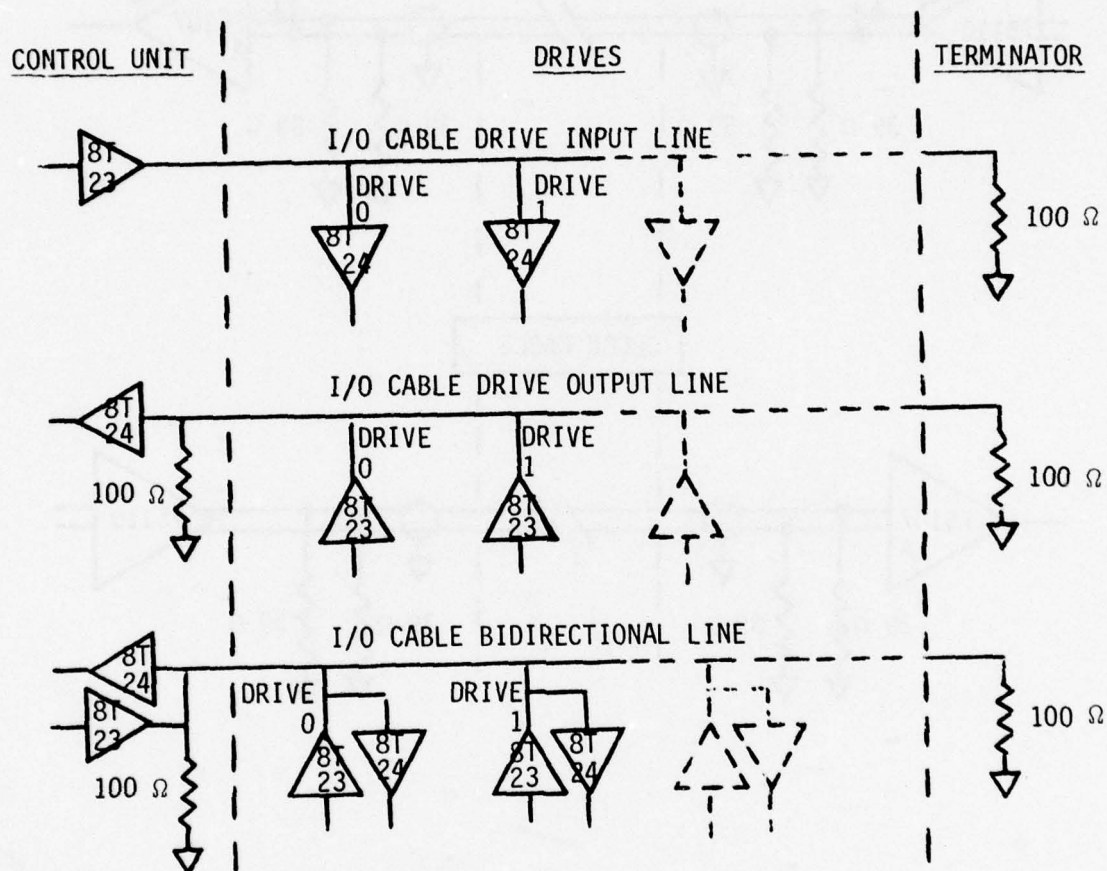


Figure 49 I/O CABLE TERMINATION

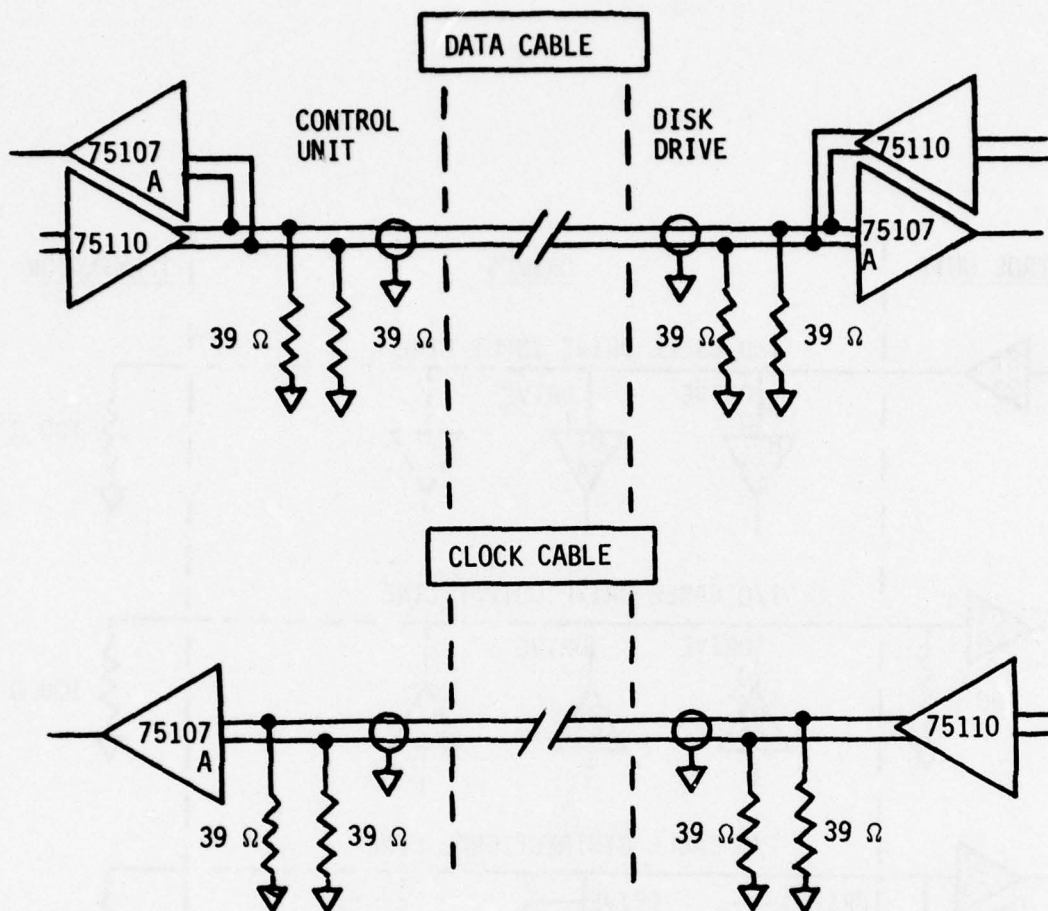


Figure 50 DATA & CLOCK CABLE TERMINATION

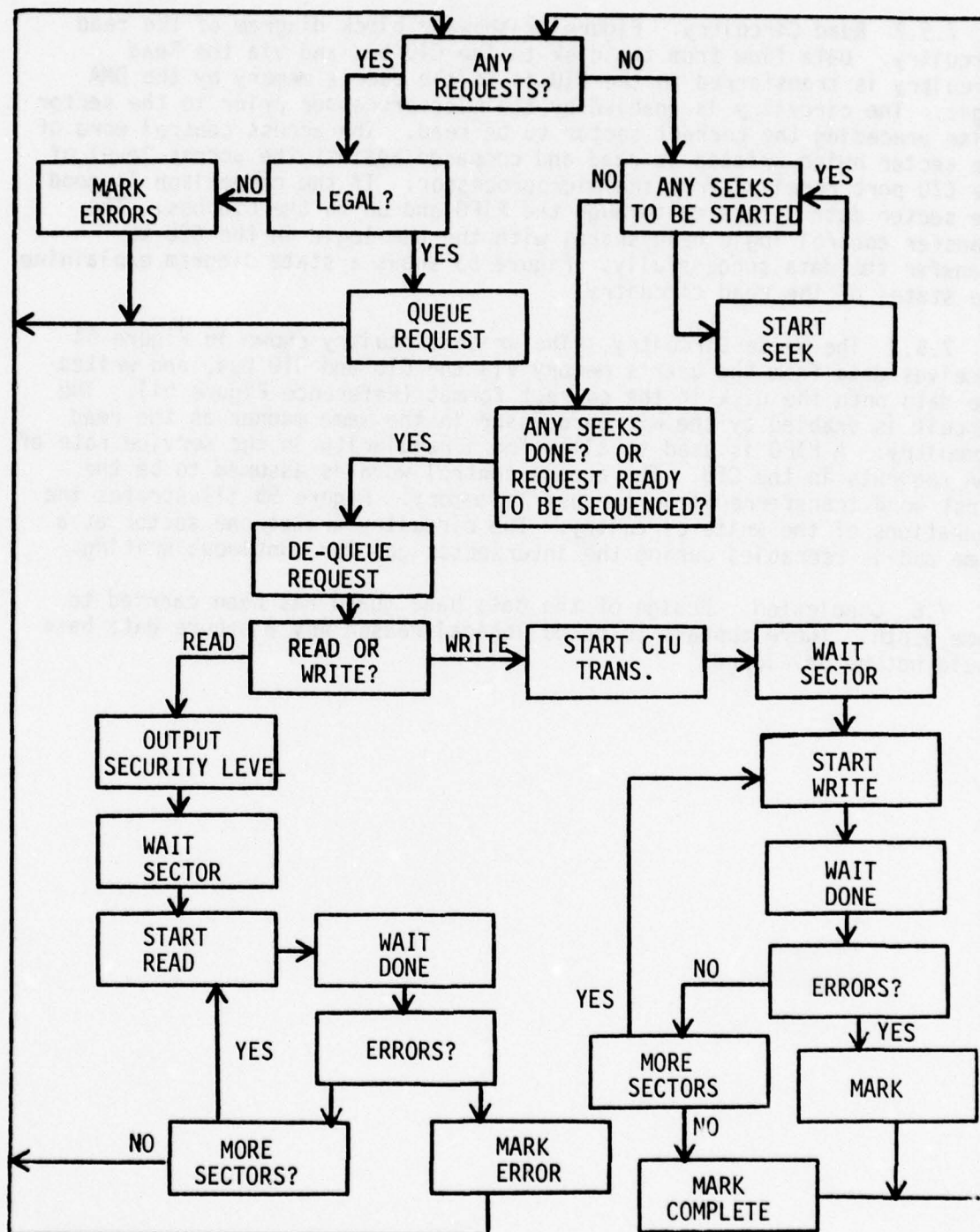


Figure 51 CONTROLLER FLOWCHART

7.5.2 Read Circuitry. Figure 52 shows a block diagram of the read circuitry. Data flow from the disk to the CIU bus and via the Read Circuitry is transferred to the CIU in to the user's memory by the DMA logic. The circuitry is enabled by the microprocessor prior to the sector pulse preceding the correct sector to be read. The access control word of the sector being written is read and compared against the access level of the CIU port received from the microprocessor. If the comparison is good the sector data is passed through the FIFO and on to the CIU bus. The transfer control logic hand shakes with the DMA logic in the CIU to transfer the data successfully. Figure 53 shows a state diagram explaining the states of the read circuitry.

7.5.3 The Write Circuitry. The write circuitry shown in Figure 54 receives data from the user's memory via the CIU and CIU bus, and writes the data onto the disk in the correct format (Reference Figure 54). The circuit is enabled by the microprocessor in the same manner as the read circuitry. A FIFO is used to allow for irregularity in the service rate of DMA requests in the CIU. The access control word is assumed to be the first word transferred from the user's memory. Figure 55 illustrates the operations of the write circuitry. The circuitry writes one sector at a time and is reenabled during the intersector gap for continuous writing.

7.6 Conclusion. Design of the data base guard has been carried to some depth. There appears to be no logical reason why a secure data base could not be developed.

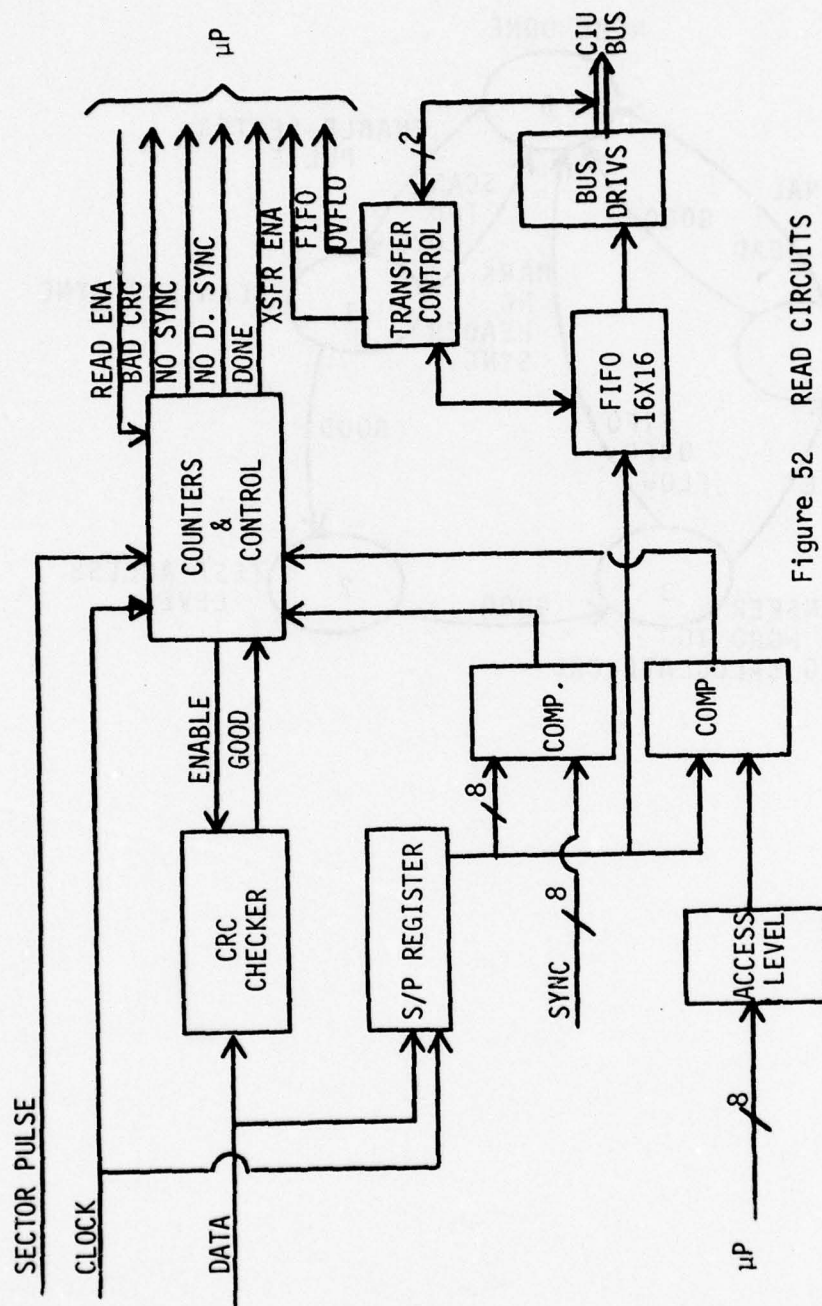


Figure 52 READ CIRCUITS

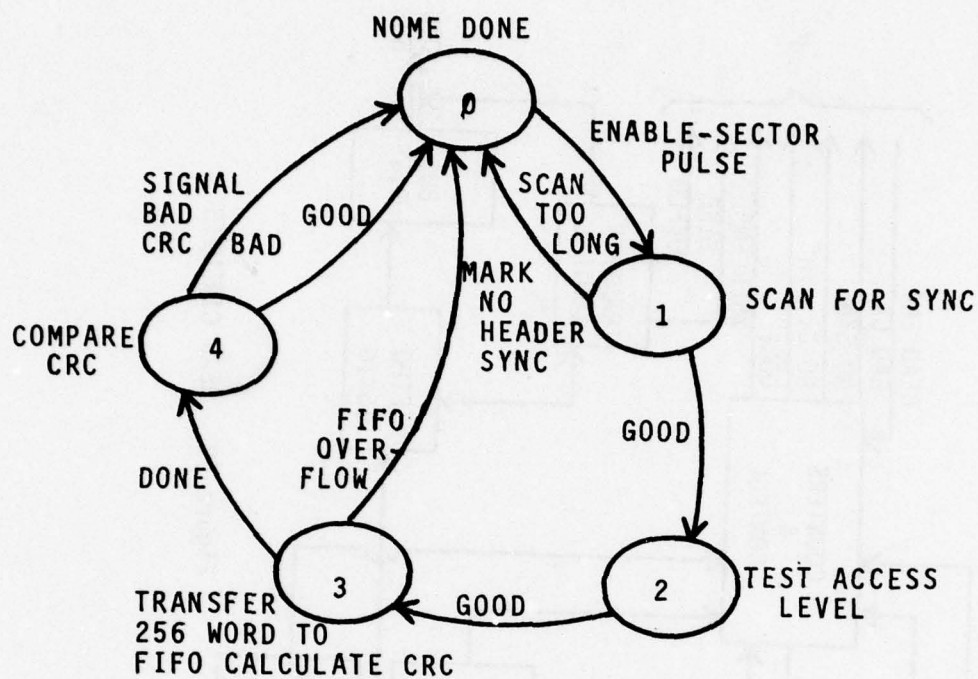


Figure 53 READ STATES

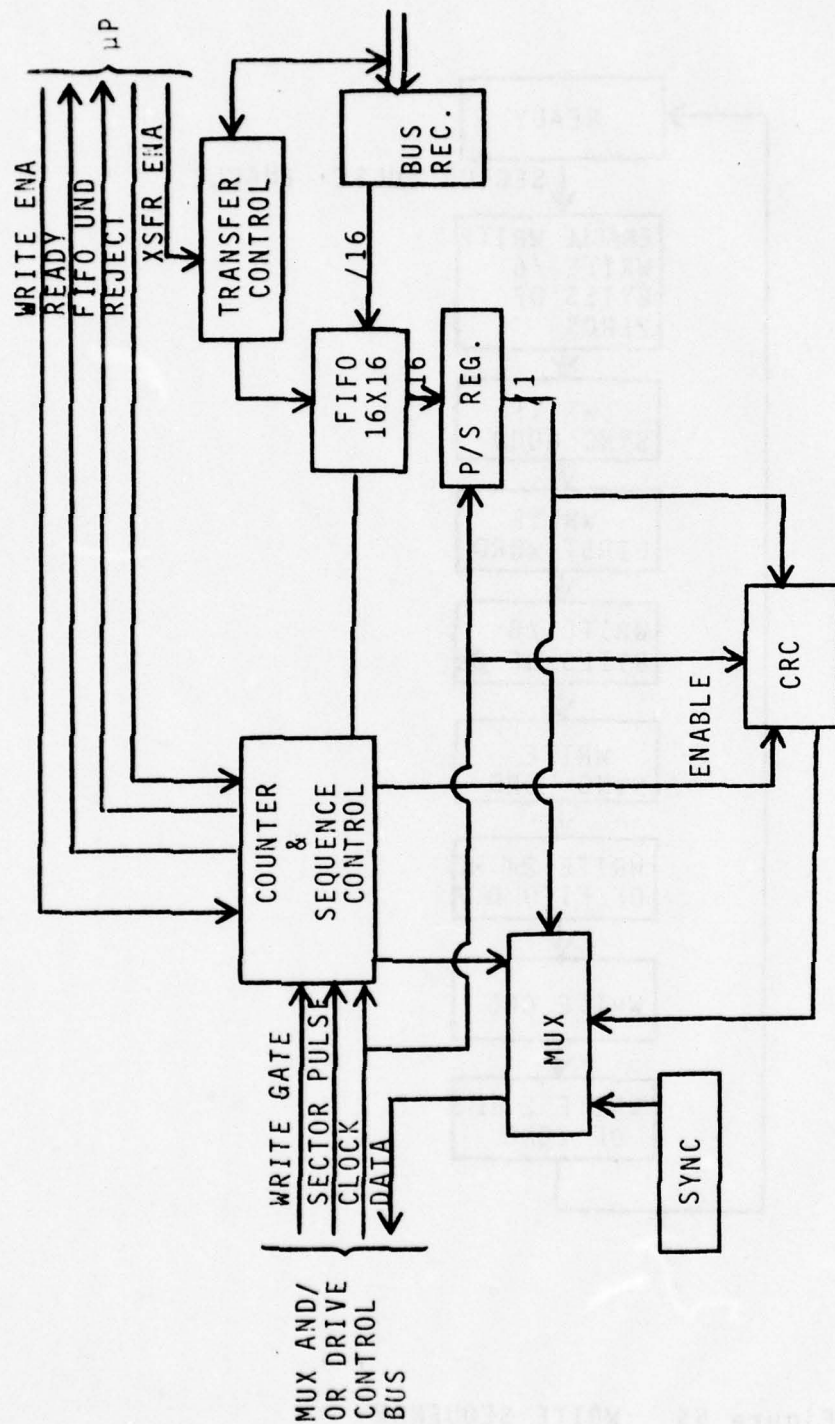


Figure 54 WRITE CIRCUIT

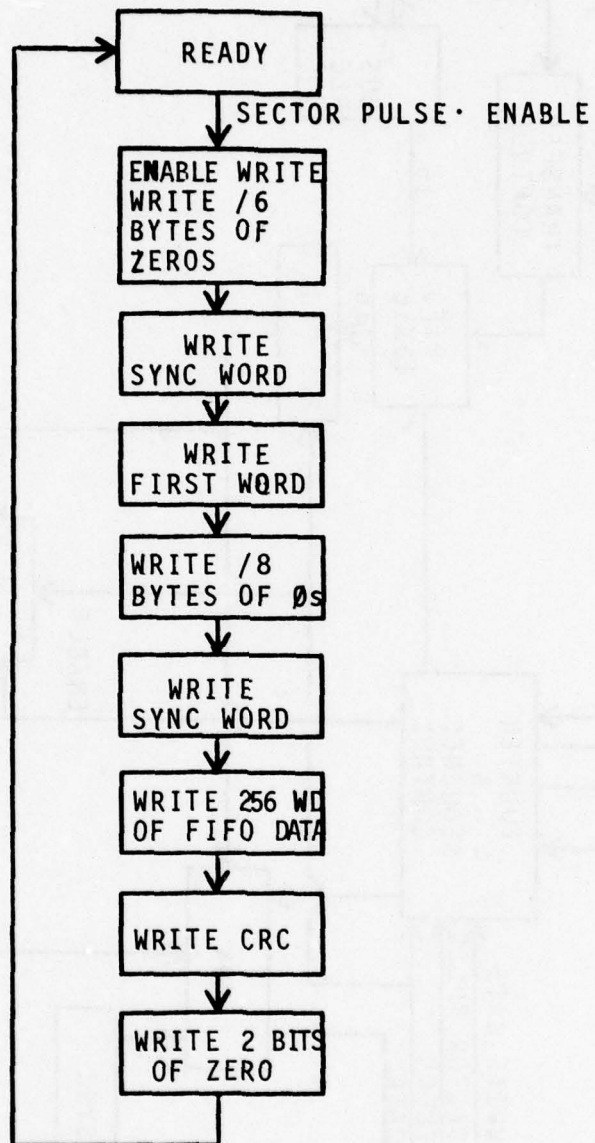


Figure 55 WRITE SEQUENCE

2.3. FINDINGS, CONCLUSIONS AND RECOMMENDATIONS

The study has shown that the system is not secure and that it is not possible to prevent the unauthorized access to the system. The system is not secure and that it is not possible to prevent the unauthorized access to the system.

The study has shown that the system is not secure and that it is not possible to prevent the unauthorized access to the system. The system is not secure and that it is not possible to prevent the unauthorized access to the system.

SECTION 8.0

FINDINGS, CONCLUSIONS AND RECOMMENDATIONS

The study has shown that the system is not secure and that it is not possible to prevent the unauthorized access to the system. The system is not secure and that it is not possible to prevent the unauthorized access to the system.

8.0 FINDINGS, CONCLUSIONS AND RECOMMENDATIONS

The study addressed the feasibility of developing a security monitoring subsystem for the AN/GYQ-21(V), interactive analyst system, IAS. We find that it is feasible to protect data in the IAS, and that at least two and possibly three approaches will accomplish that objective. The approaches and their relative merits are described as follows:

- Data Base Guard - The data base guard approach allocates one central processing unit for each security compartment. Upon completion of the sign-in procedure, the user is switched to the computer that corresponds to the user's access privilege. A Secret privilege user will be switched to a Secret computer, and will be denied access to Top Secret records in this computer. Potential vulnerabilities are the data base guard (multiported disk controller) and the initial switching mechanism. Design of the data base guard was presented in Section 7. It was shown that the microprocessor that controls communications into and out of the data base has a small program that can be certified. This will prevent the insertion of trapdoors that would defeat the protection mechanism.
The initial switching mechanism transfers the Secret user to the Secret IAS. It also represents a potential vulnerability. If the mechanism can be tricked into switching the Secret user to the Top Secret machine, the protection mechanism can be defeated. Fortunately, the microprocessor that performs the initial switching function has a small program that can be certified. We conclude that the potential vulnerabilities can be made impenetrable and as a result, the data base guard approach can be used as a basis to develop a secure IAS.
Unfortunately, the approach is not without cost penalties. Multiple computers must be used (one for each compartment). Further, the switching mechanism must be added to the system. The data base guard approach is comprised of a microprocessor costing approximately \$1500.
- Enciphered Record - The Enciphered Record approach presumes the processor is a hostile environment and applies the principles of RED-BLACK isolation the same as used in telecommunications. The records of the data base are enciphered, and even if accessed are useless without the ability to decipher them. The approach has appeal in that it is an elegant engineering solution to the problem of protecting data.
Potential vulnerabilities of the system consist of the access control mechanism, RED processor, cracking the code, and stealing the key. The access control mechanism, like that of the data base guard, is comprised of a small microprocessor with certifiable software. Alternatively, the whole mechanism may be hard wired, thereby, eliminating the software problem. The problem of isolating the RED processor was addressed in Section 7, with the

conclusion that the BLACK processor can be totally isolated from the RED processor. We have assumed throughout that a block enciphering algorithm will be used that is impenetrable. For the initial design purposes, the NBS algorithm will be used, although it is recognized that this is unacceptable for military applications. We assume the Government will supply a military-acceptable block encryption algorithm. The final way the system is defeated is by stealing the key. This can be made impossible by a number of means. One way is to manually insert the key at the guard and design the guard in such a way that if a penetration is attempted, the guard will destroy the key before anyone can gain access to it.

The sections on RED-BLACK multiprocessing and the enciphered data base system were intended to demonstrate the complexity of making this approach invulnerable. On the basis of information set forth in the preceding sections, we conclude that the potential vulnerabilities of the enciphered record approach can be made impenetrable and, therefore, the enciphered record can be used as a basis for developing an impenetrable IAS.

The enciphered record approach, like the data base guard approach, does not come free of charge. An external access control mechanism must be developed comprised of microprocessors costing approximately \$1500 per terminal. Further, because the records are enciphered and require processing, a RED processor must be added to the system. This will incur a modest addition in expense in most intelligence applications and can be accomplished by a mini-computer in most cases (one additional PDP-11, as opposed to several additional PDP-11's in the data base guard approach).

- Tag Approach - The tag approach to record security utilizes an enciphered tag to inform the exit guard of record classification. The approach is the simplest of the three and only requires an access control mechanism. Since the records are in the clear, RED-BLACK multiprocessing is not required. The approach is an effective measure against the threat of accidental disclosure. For this threat, it is the cheapest and will do the job. We, therefore, conclude that this approach is optimum against a benign threat. On the ability to withstand the attack by computer criminals, we are much less confident. As in the case of the enciphered record, potential vulnerabilities are access control mechanism, cracking the code, and stealing the key. But unlike the enciphered record approach with the data and records in the clear, the tag approach utilizes records that are in the clear. Therefore, they can be copied and dumped on a terminal or disguised as an error message and sent to the user. There are countermeasures to this vulnerability such as placing an exit guard at every terminal device and designing nonrecord communication containing an unforgeable tag, that describes the transaction as such. In practice, these may or may not be easy to implement.

There is some doubt and, therefore, we do not recommend a tag approach against the threat of malicious attack at this time.

Since, of the three possible approaches, one is at least questionable in its ability to withstand criminal attack, there remains only two possible alternatives for recommendation in its use in development of an engineering model. The data base guard approach appears the least vulnerable, but it is the most expensive. We, therefore, do not recommend it for implementation. There is a second reason for this. There is very little question of feasibility and building an engineering model of the data base guard approach would prove very little. Accordingly, we recommend that an engineering model of the enciphered record approach be developed as given in the next section.

Some experts will undoubtedly argue that building an admittedly special purpose data base system is not as productive an area of research as approaches to general purpose solutions, such as ongoing efforts to develop secure operating systems. Harris disagrees. First of all, a secure data base system would satisfy many military needs, not only in the intelligence community but also in command and control. Secondly, building special purpose machinery is an inductive approach to the general purpose problem. We have already observed that RED-BLACK multiprocessing is necessary to solve the secure data base problem. Quite possibly, a more general multiprocessing architecture will provide a basis for a multilevel secure computing system.

SECTION 9.0

SPECIFICATION OF A SECURE DATA BASE SYSTEM

9.0 SPECIFICATION OF A SECURE DATA BASE SYSTEM

9.1 Scope

9.1.1 Identification. This specification is for an Engineering Model of a Secure Data Base System (EMSDBS).

9.1.2 Functional Summary. The EMSDBS shall perform the following tasks:

- Sign-On and Sign-Off Procedures - This is an interactive communication between an operator and the system and provides the basis for preparation and termination of data base operational dialogue.
- Data Base Operational Dialogue - Provides the operator with the ability to retrieve, modify, add, and delete data base system records.
- RED-BLACK Multiprocessing - Provides secure computer-to-computer communication between two system computers.

The specification covers a model having certain security features that may be tested to establish that the enciphered record data base approach is in fact, secure.

9.2 Applicable Documents. The equipment and system software provided by the contractor shall be purchased from the Digital Equipment Corporation and is described in the following documents.

PDP-11/45 Processor Handbook
PDP-11 Peripherals Handbook
LSI-11 Processor Handbook
RSX-11M Volumes I through V
Introduction to RMS-11

9.3 Requirements. The EMSDBS shall be comprised of computing, peripheral equipment, system software and application programs. Its purpose is to provide data base communication to two or more operators in such a manner that the data base is secure. Security will be achieved by encrypting the records and data base and controlling the deciphering process.

The computing and peripheral equipment shall be as follows:

<u>Equipment</u>	<u>QTY</u>
BLACK processor, DEC, PDP-11/45	One
RED processor, LSI-11	One
Terminals for presentation and display of data base records	Two
Disk file - RK05	One
Exit guards - LSI-11	Two

Access control center - LSZ-11
Mailbox - RK05 initially

One
One

The system software shall be the RSX-11M operating system and RMS-11 records management system.

The major functions of the system are:

- Provide access to operators on and off the system
- Provide data base operational dialogue in the form of five commands; print, display, add, delete and change
- Secure communication between the RED and BLACK processors

9.3.1 Program Definition. The EMSDBS shall build upon the experience gained in the development of the Experimental, Enciphered Data Base System, described in Section 5 of this report. It will reuse concepts, design criteria, and software to the maximum extent possible. The EMSDBS will also incorporate the features of RED-BLACK multiprocessing described in Section 6.

Figure 56 shows a simplified block diagram of the EMSDBS. As in the Feasibility Model, only two terminals are used, each connected through a guard which remains transparent to communications once the user has signed on. The isolated, access control center commands the guards, verifies the identity of the user and detects any attempted sabotage. The BLACK processor contains the major portion of the software as well as the system software, RSX-11D and the data base management software RMS-11. It is a major processing element and controls all access to the data base. The latter is a disk file containing enciphered variable length records. The BLACK processor communicates to the RED processor by a mailbox. This design is described in Section 6, RED-BLACK Multiprocessing, of this report. The processing is required to demonstrate that it is feasible to achieve security while still deciphering records for processing.

Table 24 shows the utilization of equipment during the seven types of transactions that the user may execute from a given terminal. The transactions are described as follows:

- Sign-On - To gain access to the computing system, the user must sign-on. The user enters the code that identifies a sign-on procedure to the guard. The guard communicates control to the access control center in charge of executing the sign-on and sign-off process. The user is identified and requests access to the data base. The access control center verifies identity by commanding the user to enter the password. After this is successfully accomplished, the access control center is satisfied with the user identity and checks the access privileges of that user, either Secret or Top Secret. If the user has Secret privilege only, that information is transferred from the access control center to the guard by way of a command stating that only Secret records will be passed to that terminal user. As shown in

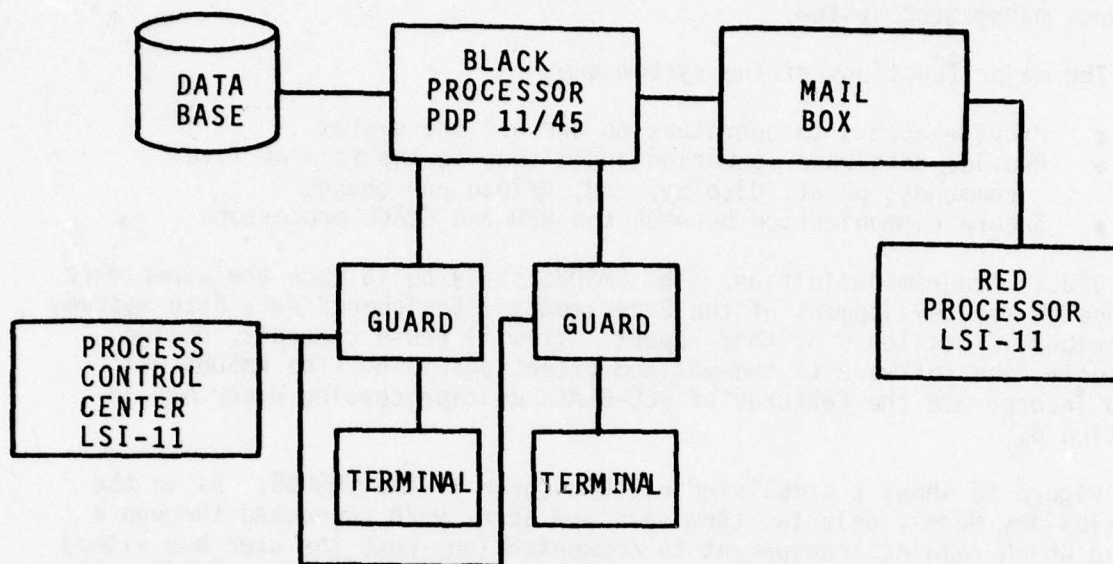


Figure 56 DATA CONTROL

Table 24. Function/Equipment Matrix

Function	Equipment					
	Terminal	Guard	Access Control	Black Processor	Red Processor	Data Base
Sign-On	X	X	X			
Sign-Off	X	X	X			
Display	X	X		X		X
Print	X	X		X		X
ADD	X	X		X	X	X
Change	X	X		X		X
Delete	X	X		X		X

the table, the sign-on procedure involves the terminal and guard as to all seven transactions; however, the only additional equipment involved is the access control center.

- Sign-Off - This transaction simply terminates the user's time on the terminal and prevents a second user from gaining access with the same privileges as the preceding user. It also involves the same equipment as the sign-on procedure.
- Display - The command formats are described in Section 5 of this report. Briefly, display is a command that requests a particular record be presented to the terminal user. The request is via the terminal and guard, to the BLACK processor, which queries the data base and returns the record matching the query parameters. The record is returned to the guard for verification of the record classification. If the record is Secret, it is deciphered and passed on to the user. If the record is Top Secret, the user denied access the record is destroyed, and the access control center is notified that a potential breach in security has occurred.
- Print - This command is very similar to Display.
- ADD - This command adds a record to the data base. The format is described in Section 6 of this report. To test the feasibility of RED-BLACK processing, the add command is assumed, not only to result in a new record being added to the data base, but also that all terminal users be notified that the new record and an abstract of its contents have been added. The additional record created by the terminal user is enciphered by the guard before it is communicated to the BLACK processor. Therefore, the BLACK processor cannot process the record to obtain the abstract. The

BLACK processor takes two actions; it inserts the record into the data base and secondly, it communicates the enciphered record to the RED processor with instructions to calculate an unclassified abstract to the record for communication to the user. The communication between the BLACK processor and the RED processor is via the mailbox. The RED processor completes the abstract and returns the results to the BLACK processor for communication to the terminals. Table 24 shows that the ADD transaction utilizes all the equipment except the access control center.

- Change - This command results in the contents of a record being changed by the terminal user. The change record is enciphered by the guard before it is passed to the BLACK processor for replacement. The flow of information is from the terminal and guard, to the BLACK processor, to the data base.
- Delete - This transaction deletes the record from the data base. The information flow, as shown by the equipment utilized in Table 24, is the terminal, the guard, the BLACK processor, and the data base.

Since the model is for engineering purposes only, the timing is of no consequence. Accordingly, no timing specifications are set forth.

The major functions of the computer program fall into four major categories as follows:

- Guard Program - The Guard Program is described in Paragraph 5.2 of this document.
- Access Control Center Program (ACC) - Figure 57 shows the overall program for the access control center. After it is initialized, the program checks the incoming lines from the two guards to detect the sign-on procedure. If a sign-on procedure has been completed by an operator, the ACC program proceeds to verify the identity of the user, look up the access privileges, and command the guard to pass records within that access privilege. If there are no sign-on requests, the program checks for sign-off procedures. If such a procedure is detected, the access control center clears the guard of its current access privileges, reinitializes, and returns to the beginning of the program. If no sign-off procedure is detected, the program proceeds to check for errors. An error is encountered when a Secret terminal has requested a Top Secret record. If no errors are detected, the program returns to its beginning point. If an error is detected, a processing algorithm is entered before returning control to the beginning of the program.
- BLACK Processor Program - The BLACK Processor program has been described in Paragraph 5.3 of this document.
- RED Processor - Figure 58 shows the flow diagram of the RED Processor program after initialization. The program continuously searches the mailbox for an ADD transaction from a user. This is the only transaction that requires the aid of the RED

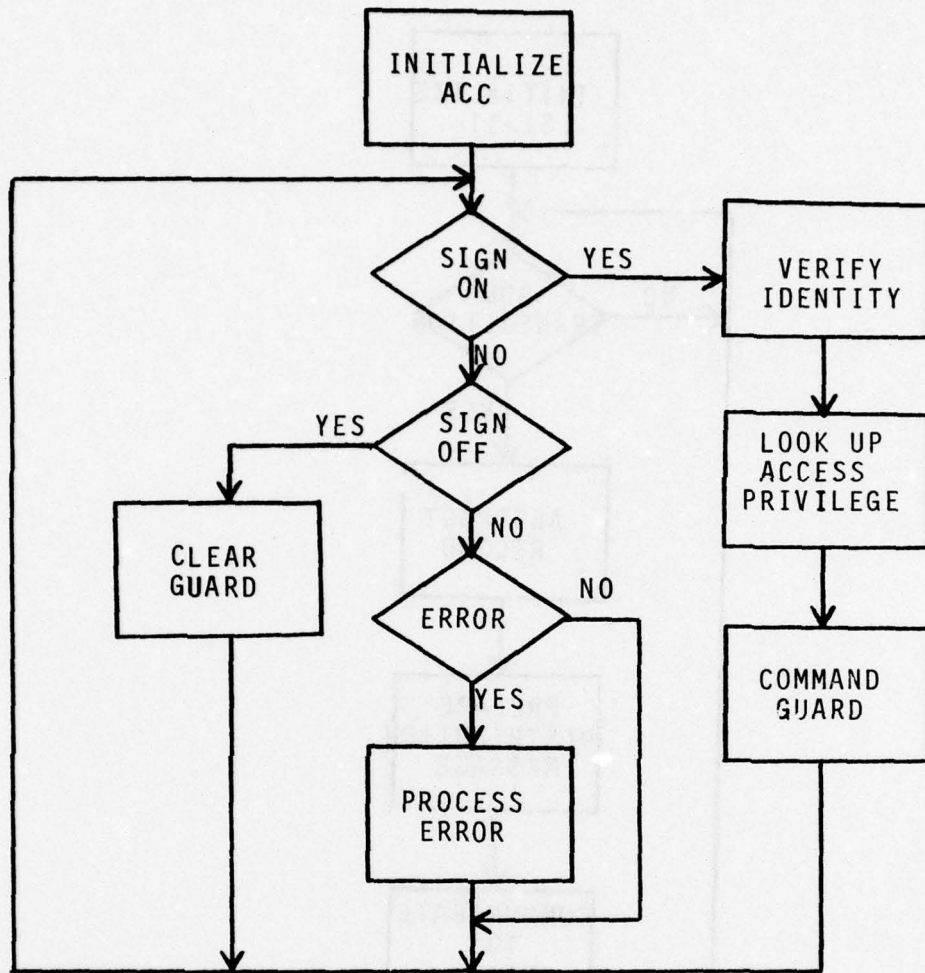


Figure 57 ACCESS CONTROL CENTER

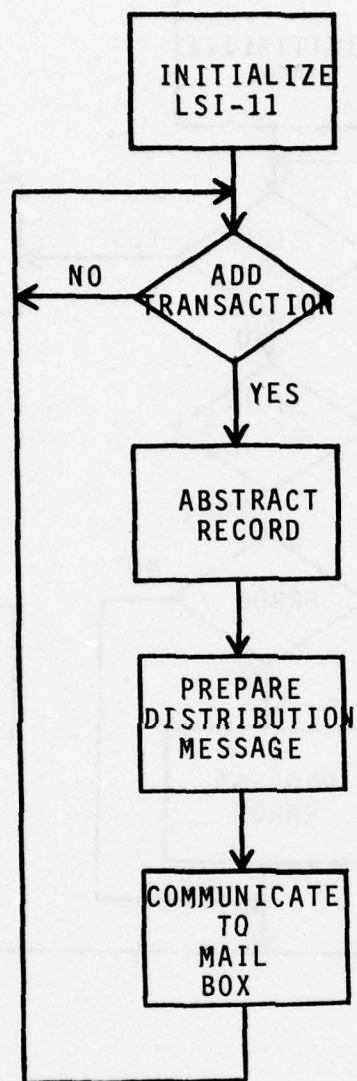


Figure 58 RED PROCESSOR PROGRAM

processor. When an ADD transaction is encountered, the record is abstracted and messages are prepared for distribution to the two terminals. The messages are communicated to the mailbox for distribution and the program returns to its beginning point.

9.3.2 Detailed Functional Requirements. The inputs, outputs, and processing for the four types of programs are:

- Guard Program - Reference Paragraph 5.2.1 of this report.
- Access Control Center Program - The inputs, outputs, and processing are to be determined.
- BLACK Processor - Reference Paragraph 5.3.1 of this report. These programs will also interface to RSX-11M. See "Introduction to RSX-11M."
- RED Processor - Inputs, outputs, and processing to be determined.

9.3.3 Adaptation. The details on the data requirements for the secure data base system are described in "Introduction to RSX-11M."

9.4 Quality Assurance Provisions

9.4.1 Introduction. The size of the programs dictates that development will take place on a set of modules integrated into subprograms and programs. Examples of the development work and listings are shown in the appendix. The guard programs, access control center programs, and red processor programs will be developed as separate entities. The black processor programs are more complex, requiring interface with RSX-11M and RMS-11. System tests will integrate all of the programs into an operational system.

9.4.2 Test Requirements. Testing will proceed at the module, subprogram and program level. Final tests will be based upon interactive dialogue between the data base and the operator.

9.4.3 Acceptance Test Requirements. The operations system will be demonstrated by a user/query response, as specified in the interactive dialogue described in Section 5 of this report. The contractor will prepare and submit an acceptance test for the buyer's approval. The buyer will witness the acceptance.

Security testing will begin following acceptance of the FMSDBS as an operational system. A test plan will be prepared to examine the security of the data bus system.

9.5 Preparation For Delivery. The EMSDBS will be installed at the contractor's facility where acceptance testing will occur. Demonstrations of feasibility will also occur at the contractor's site. It is not anticipated that the EMDBS would be shipped to a Government facility.

APPENDIX A
PROGRAM LISTINGS

COPY AVAILABLE TO EDO DOES NOT
PERMIT FULLY LEGIBLE TRANSCRIPTION

COPY AVAILABLE TO EDO DOES NOT
PERMIT FULLY LEGIBLE TRANSCRIPTION

A-1

SJNR DATABASE RLD ON DK1
DATE:-17-AUG-77
TIME:-00:23:08
SPIN PTD
PTP V10-03A
*CONPOL.001/DF
*RPN.SRC/DF
*CONPOL.001CONPOL.ISS
*RPN.SRCRT:/FA
SEND
*
SPIN .JOYIAL


```

JOVIAL ISS
* HARRIS JOVIAL COMPILER
---VERSION -3A
PAGE 1
'' THIS PROGRAM READS EVENT RECORDS FROM THE CARD READER AND
'' STORES THEM ON THE DATABASE DISK FOR USE BY THE ISS SYSTEM
I = 0
START:TRACE
DIRECT $
  .EVEN
  .MACRO STMT NO. ?A1
  .GLOBL STMTNO
  MOV SNO,STMTNO
  .GLOBL TRACE
  JSP R5,TRACE
  RP A1
  .WORD STMTNO
  .ENDM
JOVIAL
DIRECT $
OVER: JSP R5,PCD ; READ NAME OF EVENT
IF JCARD(SOS) EQ ATCHR $ STOP $
CSMOV (30,ANAMP,ACARD,1) $
READ (R,PCDF1) LATITUDE, LONGITUDE, EVENTTYPE, COUNTRY, TIME, REPORT'NO
DIRECT $
JSP R5,PCD ; READ CASE'NO, COMMENTS, CTAG'E
CSMOV (R,CTAG'E,30,ACOMMENTS,12,ACASFINO,ACARD,3) $
'' NOW EVENT IS STORED IN COMPOOL, TRANSFER TO DISK ''
DRTN (AEVENT) $
GOTO OVER $
PCDF1. FORMAT (2F10.4,2I1,F10.4,1I0) $
DIRECT $
  .CALLC -INIT..TRAN,..WAIT
  .GLOBL DRTN
  MSTK = $5
OKTAN:
  .INIT #DK1 ; INIT LINK BLOCK
  LDF (MSTK)+,ACD ; CONVERT ADDR OF EVENT TO FIXED
  STCFT ACD,-(MSTK) ;
  TST (MSTK)+
  MOV (MSTK)+,TRANBLK+2 ; STORE ADDR OF EVENT IN TRANBLK
  .TRAN #DK1,TRANBLK ; WRITE TO DISK
  .WAIT #DK1 ; WAIT UNTIL I/O IS DONE
  INC TRANBLK ; INC BLOCK # FOR NEXT RECORD
  RTS PC
  .WORD 0 ; ERROR RETURN
  .WORD 0 ; LINK POINTER
  .PAND0 / ; LOGICAL NAME OF DATASET
  .RVE 1,1 ; NUMBER OF WORDS, UNIT #
  .PAND0 /DK/ ; PHYSICAL DEVICE NAME
  .PAND0 2400. ; STARTING BLOCK #
  .WORD 0 ; STARTING ADDR IN CORE
  .WORD 256. ; NUMBER OF WORDS
  .WORD 2 ; WRITE
  .WORD 0 ; FOR MONITOR USE
TRANBLK:

```


DATA BASE REFERENCE LISTING

S	5	13	0	0
CARD	0	14	1	40
ICARD	0	14	0	8
ATCHR	75	9	0	8
EVENT	6501	2	1	80
NAME	6501	14	0	240
LATITUDE	6520	11	0	32
LONGITUDE	6522	11	0	32
EVENTTYPE	6524	9	0	8
COUNTRY	6524	9	0	8
TIME	6525	9	0	32
REPORT NO	6527	9	0	16
CASE NO	6530	9	0	96
COMMENTS	6536	9	0	240
CTAG F	6555	9	0	64
I	1	13	0	16

COMPONL SPACE USED = 1098

0 ERRORS

AD-A054 508

HARRIS CORP MELBOURNE FLA ELECTRONIC SYSTEMS DIV
INTELLIGENCE SECURITY SUBSYSTEM.(U)
MAR 78 F ANDERS, W MALL, R MCGILL

F/G 9/2

UNCLASSIFIED

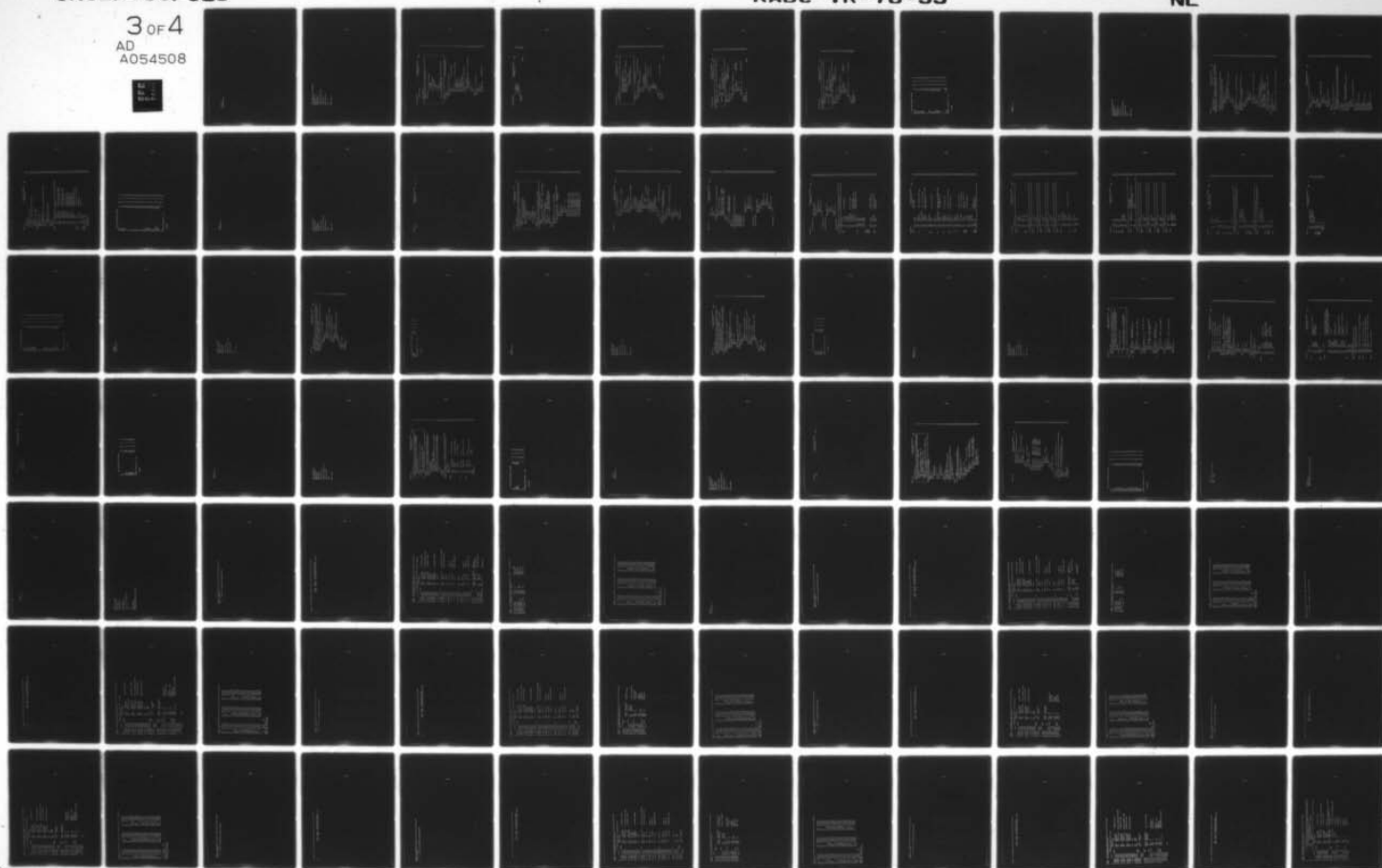
RADC-TR-78-33

F30602-76-C-0445

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3 of 4

AD
A054508



A-6

SJ04 COMPILE ISS SUBROUTINES

DATE:-17-AUG-77

TIME:-00:24:26

SRUN PTP

PIP V10-03A

#COMPOL.001/DF

#COMPOL.001<COMPOL.ISS

#RPN.SRC/DF

#RPN.SRC<RI:/FA

SEND

#

SRUN JOVIAL


```

ISS SUBROUTINES          * HARRIS JOVIAL COMPILER          PAGE 1
PROGRAM ISSRMS          S      ---VERSION -3A
LCP SUBROUTINE          S
ROUTINE TO STORE OR FETCH A COMPOOL ENTRY
INPUTS ARE :
FUN = FUNCTION TO PERFORM
      = 0 FETCH
      = 1 STORE
TEPR = ERROR CONDITION
      = 0 NO ERROR
      = 1 ERROR
A = TYPE
A = FP
C = NR
D = ADDRESS
TAG = ADDRESS OF RYTF STORAGE, NTAG = LENGTH
OUTPUTS ARE THE ABOVE ITEMS SPT
IFPR = 0
IF FUN EQ 1 S
  THEN
    CALL SCP S " SEARCH COMPOOL. "
    IF TEPR EQ 0 S
      THEN
        IFPR = 1 S
        ELSE S
          IFPR = 0 S
          " PUT DATA IN COMPOOL. "
          TYP (STMENTS) = A S
          DEF (STMENTS) = 0 S
          TPR (STMENTS) = B S
          INP (STMENTS) = C S
          ADD (STMENTS) = D S
          DOTNT (STMENTS) = NSYM S
          NCHAP (STMENTS) = NTAG S
          INENT = INENT + 1 S " STEP INDX "
          T = 0 S
          DO WHILE T LS NTAG S
            SYM(NSYMS) = TAG(SIS) S " MOVE IN SYMBOL "
            NSYM = NSYM + 1 S
            T = T + 1 S
          END DO S
          END IF S
          RETURN S
        ELSE S
          CALL SCP S " SEARCH COMPOOL. "
          IF TEPR EQ 1 S
            THEN
              RETURN S
            ELSE S
              A = TYPE(SIS) S
              DEF(SIS) = 1 S

```

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```

ISS SUBROUTINES
*
P = YFR(SIS) $
C = INR(SIS) $
D = ADR(SIS) $
END IF $
END IF $
RETURN $

* HARRIS JOVIAL COMPILED
---VERSION -3A
PAGE 2
PAGE 8
34
35
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40

```

[illegible]


```

ISS SUBROUTINES                                *  HARRIS JOVIAL COMPILER  PAGE 4
-----VERSION -3A-----
''-----''
OCTI SUBROUTINE S
'' ROUTINE TO CONVERT AN OCTAL STRING TO AN OCTAL BINARY NUMB ''
'' INPUTS ARE: ''
'' ICARD = IMAGE ''
'' ICOL = STARTING COLUMN ''
'' OUTPUTS ARE: ''
'' ICOL = POINTS TO FIRST NONOCTAL COL ''
'' SUM = CONVERTED RESULT ''
''-----''
ITEM OCTI T 1 1 S '' END INDICATOR ''
SUM = 0 S
OCTE = 0 S
DO WHILE OCTE EQ 0 S
  I = 0
  DO WHILE T IS R S
    IF ICARD(ICOL) EQ IDEC(SIS) S
      THEN
        SUM = SUM * 8 + T
        ICOL = ICOL + 1 S
      ELSE S
        I = I + 1 S
      FND IF S
      IF I GO R S OCTE = 1 S ''SET DONE FLAG ''
    FND DO S
  FND DO S
  RETURN S
END SUBROUTINE S

```

PAGES

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72
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```

ISS SUBROUTINES          *  HAPPIS JAVIAL COMPILER          PAGE 5
-----
UDII SUBROUTINE $
  ROUTINE TO CONVERT A DECIMAL STRING TO A DECIMAL BINARY NUMB
  INPUTS ARE:
    TCADD = YNAGE
    TCOL = STARTING COLUMN
  OUTPUTS ARE:
    TCOL = POINTS TO FIRST NON-DECTMAL COL
    SUM = CONVERTED RESULT
  IFM UDIF J 1 U $      END INDICATOR
  SUM = 0 $
  UDIE = 0 $
  DO WHILE UDIE EQ 0 $
    I = 0
    DO WHILE T LS 10 $
      IF ICAPD(SICOL) EQ IDFC(SIS) $
        THEN
          SUM = SUM*10 + I
          TCOL = TCOL+1 $
        ELSE $
          T = T + 1 $
        END IF $
        IF T GO 10 $ UDIE = 1 $      SET DONE FLAG
      END DO $
    END DO $
  RETURN $
END SUBROUTINE $
END PROGRAM $

```

01
 02
 03
 04
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DATA BASE REFERENCE LISTING

S	5	13	0	0
ICARD	0	14	0	0
INFC	67	14	0	0
ICOL	106	0	0	16
TYPE	112	0	0	16
SUM	115	0	0	16
FIN	117	0	0	16
IERR	120	0	0	16
NTAG	122	0	0	16
NSYM	123	0	0	16
A	124	0	0	16
B	125	0	0	16
C	126	0	0	16
D	127	0	0	16
INENT	131	0	0	16
TAC	170	14	0	0
TYP	2057	9	0	4
REF	2057	9	4	1
IFR	2057	9	5	5
INR	2057	0	10	6
NCHAR	3043	9	0	5
POINT	3043	9	5	11
ADR	4027	0	0	16
SYM	5013	14	0	0
I	1	13	0	16
J	2	13	0	16
K	3	13	0	16
L	4	13	0	16
OCIE	6746	9	0	1
UDIE	6746	9	0	1

COMPOOL SPACE USED = 1123

0 ERRORS

A-13

SPINISH
TIME:-00:31:37

A-14

SJNR COMPILE COMPOL READ
DATE:-17-AUG-77
TIME:-00:31:40
SRUN PTP
PIP V10-03A
#COMPOL.001/DE
SRPN.SPC/DF
#COMPOL.001<COMPOL.ISS
SRPN.SRC<RI:/FA
SEND

SRUN JOVIAL

```

JUVIAL ISS                                * HARPIS JUVIAL COMPTIER          PAGE 1
LCMBL SUBROUTINE S
  " SUBROUTINE LCMBL - LOAD COMPOOL INTO SHARED MEMORY. THIS PROGRAM "
  " READS THE DISK AND FINDS THE FILE - COMPOOL.001 - AND LOADS IT INTO "
  " THE PROPER PLACE IN THE COMPOOL IN SHARED MEMORY
  I = 0 S
  DSKRW(ADISK'RUUF,2,512) S " READ WFD BLOCK INTO BUFFER "
  I = 1 S " SET INDEX TO 1, SKIP WFD LINK PTR "
  DO UNTIL DISK(ETS) EQ 0 S " CHECK ALL WFC S "
    IF DISK(ET+25) EQ 2 S
      THEN S
      IF DISK(ET+15) EQ 1 S
        THEN S " FOUND 1,2 WFC "
        J = DISK(ET+15) S " SAVE WFD START BLK "
      ELSE S
      END IF S
      ELSE S
      I = I + 4 S
    END IF S
  END DO S
  NEXT. DSKRW(ADISK'RUUF,1,512) S " READ WFD START BLOCK "
  NXT1. TT = 0 S
  TL = ADISK(ETS) S
  CHKEN(OT1,OT1) S " CHECK FILENAME FOR COMPOOL.001 "
  IF TT GR 0 S " THEN NO MATCH "
    THEN S
    I = I + 4 S
    IF I GR 254 S
      THEN S
      IF DISK(ETS) EQ 0 S
        THEN S
        CALL FRM S
        ELSE S
      END IF S
      J = DISK(ETS) S " SET J TO NEXT WFD BLOCK "
      GOTO NEXT S
      ELSE S
      GOTO NXT1 S
    END IF S
    ELSE S " FOUND CORRECT ENTRY "
    I = I + 4 S " FOUND CORRECT ENTRY "
    FRD = DISK(ETS) S " BYTE COUNT OF LAST BLOCK "
    SKIP = DISK(ET+15) S " START BLOCK "
    LENGTH = DISK(ET+25) S " LENGTH "
    FRM = DISK(ET+35) S " END BLOCK "
  END IF S
  " BEGIN TO LOAD FILE COMPOOL.001 INTO SHARED MEMORY "
  TJ = 0 S " INDEX TO ENTRY "
  J = SALX S
  OVER. DSKRW(ADISK'RUUF,J,512) S
  TK = 0 S
  I = 511 S
  IF DISK(ETS) EQ 0 S L = FRD-1 S " BYTE COUNT OF LAST BLOCK "

```



```

JOVIAL ISS
OVR. IF TK GO 1 S ' ' END OF SECTOR OR FILE ' '
    THEN S
    IF DISK(SOS) EQ 0 S
        THEN S
        GOTO OUT S
        ELSE S
    END IF S
    J = DISK(SOS) S
    GOTO OVER S
    ELSE S
    IF TJ EQ 37 S ' ' PROCESS CARD IMAGE ' '
        THEN S
        CALL PLING S
        TJ = 0 S
        ELSE S
    END IF S
    FWTAP(STJS) = DISK(STKS) S
    TJ = TJ + 1 S
    TV = TK + 1 S
    END IF S
    GOTO OVER S
    ' ' FINISH READING AND STORING FILE ' '
    RETURN S
    PLING SUBROUTINE S
    ' ' THIS SUBROUTINE TAKES THE CARD IMAGE THAT HAS BEEN LOADED ' '
    ' ' INTO FWTAP AND LOADS THAT COMPOU DATA INTO THE SCAPED MEMORY ' '
    T1 = TT1 S
    T2 = TT2 S
    T3 = TT3 S
    T4 = TT4 S
    T5 = TT5 S
    TM = 10 S ' ' INDEX FOR 1ST 15 STRING ' '
    CALL LOADC S ' ' LOADS DEC STRING INTO CARD FOR CDCON ' '
    CALL CDCON S
    IF DCR EQ 0 S
        THEN S
        CALL FRM S
        ELSE S
        VTAG = SUM S ' ' STORE CONVERTED RESULT ' '
    END IF S
    TM = 15 S
    CALL LOADC S
    CALL CDCON S
    IF DCR EQ 0 S CALL FRM S
    A = SUM S
    TM = 20 S
    CALL LOADC S
    CALL CDCON S
    IF DCR EQ 0 S CALL FRM S
    R = SUM S
    TM = 25 S
    CALL LOADC S
    CALL CDCON S
    IF DCR EQ 0 S CALL FRM S
    C = SUM S

```

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JOVIAL: YSS
HARRIS JOVIAL COMPILER
---VERSION -3A
PAGE 3

TN = 10 S
CALL LOADC S
CALL CCON S
IF CCON EQ 0 S CALL ERRO S
0 = CCH S
** NOW HAVE VALUES LOADED FOR LCP TO WORK **
FIN = 1 S
CALL LCP S
IF NTAG EQ 1 S GOTO LOOP2 S
RETURN S

LOOP2: IF T1 EQ AT S GOTO OUT S
RETURN S

END SUBROUTINE S
RETURN S

LOADC SUBROUTINE S
** THIS ROUTINE LOADS A DECIMAL STRING INTO CARD FOR CCON **
TCOL = 0 S
TN = 0 S
DO UNTIL TN GO S
  TCARD(STNS) = FWTDF(NTN+TMS) S
  TN = TN + 1 S
END DO S
RETURN S
DIRCT S

.CCCHL CHCKV
CHKV: ; THIS ROUTINE COMPARES 3 RAD50 WORDS WITH FILENAME COMPOU.001
      MOV R0, -(SP)
      MOV R1, -(SP)
      LDF (MSTK)+, ACO
      STGT ACO, -(MSTK)
      TST (MSTK)+
      MOV (MSTK)+, R0
      LDF (MSTK)+, ACO
      STGT ACO, -(MSTK)
      TST (MSTK)+
      MOV (MSTK)+, R1
      CVD FINV1, (R1)
      RVE NATCH
      CVD FINV2, 2(R1)
      RVE NATCH
      CVD FINV3, 4(R1)
      RVE NATCH
      MOV #1, R0
      MO R0
      NATCH: CLP R0
      MD: (SP)+, R1
      MOV (SP)+, R0
      RTS PC
      FINV1: .RAD50 /CONV/
      FINV2: .RAD50 /DNI/
      FINV3: .RAD50 /OOI/
      JOVIAL
      END SUBROUTINE S
      END PROGRAM S

; SAVE REG
; STORE AND CONVERT ADDRESS
; TO RETURN RESULT, DEF, 1ST
; STORE ADDR IN R0
; OF 1ST RAD5/ WORD
; STORE ADDR IN R1
; COMPARE 1ST 3 CHAR
; RD IF NO MATCH
; COMPARE 2ND 3 CHAR
; RD IF NO MATCH
; COMPARE 3RD 3 CHAR
; RD IF NO MATCH
; SET RESULT TO 1 FOR TRUE
; SET RESULT TO 0 FOR FALSE
; RESTORE REG
; RETURN

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DATA BASE REFERENCE LISTING

S	ICARD	5	13	0
AI		0	14	0
ICOL		54	14	0
SIIM		106	9	0
SIIM		115	9	0
FIIM		117	9	0
NTAG		122	9	0
A		124	9	0
P		125	9	0
C		126	9	0
D		127	9	0
T1		170	9	0
T2		171	9	0
T3		172	9	0
T4		173	9	0
T5		174	9	0
DCR		573	9	0
TI		604	9	0
TJ		605	9	0
TK		607	9	0
TL		610	9	0
TM		611	9	0
TN		612	9	0
SRIK		631	9	0
FRP		632	9	0
LENGTH		633	9	0
FR1K		634	9	0
FMTBF		648	14	0
TT1		645	9	0
TT2		646	9	0
TT3		647	9	0
TT4		650	9	0
TT5		651	9	0
DISK RUFF		5777	2	1
DISK8		5777	14	0
DISK		5777	9	0
I		1	13	0
J		2	13	0
L		4	13	0
COMPOOL. SPACE USED = 1143				

COMPOOL SPACE USED = 1143

0 ERRORS

A-19

SPINTSH
TIME:-00:36:53

A-20

5100 CCYC COMPLE

DATE:-22-AUG-77

TIME:-00:00:15

SRUN DIP

PIP V10-03A

SRPN_SPC/DF

*COMPRI.001/DF

*COMPRI.001COMPRI.ISS

SRPN_SPCARI:/FA

SEND

*

SRUN JOVTAL

JOVIAL TSS

PAGE 8

* HARRIS JOVIAL COMPILER
---VERSION -3A

PAGE 1

1


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JUVIAL INS
* HARRIS JUVIAL COMPILER
---VERSION -3A
PAGE 2

CCXFC SUBROUTINE S
-----
!! CODE EXECUTION - CAPTURES OUT THE PRESCRIBED OPERATIONS OF THE
!! GENERATED POLISH STRING
!! INPUTS ARE:
!! POLSTK = CONTAINS POLISH TARGET STRING
!! (ACCESSED BY PNTSV(PINDEX) )
!! MSTK = USED AS OPERAND STACK HERE
!! MVTYP = WITH ACTION TYPE
!! = 1 = DISPLAY
!! = 2 = PRINT
!! = 3 = DELETE
!! = 4 = ADD
!! = 5 = CHANGE
!! MSTYP = WITH SUBJECT TYPE
!! = 1 = EVENT
!! = 2 = REPORT
!! OUTPUTS ARE:
!! RESULTS OF CODE EXECUTION (DEPENDENT ON COMMAND)
-----
IF MVTYP EQ 1 S
!! SET DISK SECTOR RASE !!
THEN S
!! EVENT !!
K = NDEVENT S
RCPCON = NENT(EVENT) * NUSEN(EVENT) S "BYTE COUNT-EVENT"
ELSE S
!! REPORT !!
RCPCON = 512 S " BYTE COUNT - REPORT "
J = 2400 S " DISK SECTOR RASE - REPORT "
K = NREPORT S " NUMBER OF REPORT RECORDS "
END IF S
I = 0 S
DO UNTIL, T GO K S
  DSKRQ (RCPCON,J,DISKIRUF) S " READ RECORD "
  M = 0 S
  DO UNTIL, GO (PINDEX - 1) S " EXECUTE POLISH STRING "
    IF PNTSV(M) EQ ESCHP S " OPERATOR "
      THEN S
      M = M + 1 S
      TI = PNTSV(M) S
      IF TI, EQ A S
        THEN S
        CALL IFOP S " IF "
      ELSE S
      END IF S
      IF TI, EQ 7 S CALL ADDOP S " AND "
      IF TI, EQ 8 S CALL OPOR S " OR "
      IF TI, EQ 9 S CALL NOTOP S " NOT "
      IF TI, EQ 10 S ARV(CTYP) S " EQ "
      IF TI, EQ 11 S ARV(CTYP) S " NE "
      IF TI, EQ 12 S ARV(CTYP) S " IF "
      IF TI, EQ 13 S ARV(CTYP) S " CF "
      IF TI, EQ 14 S ARV(CTYP) S " LT "
      IF TI, EQ 15 S ARV(CTYP) S " GT "
      IF TI, EQ 16 S ARV(CTYP) S " + "
      IF TI, EQ 19 S ARV(CTYP) S " - "

```

JOURNAL YES

PAGE 3

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40      IF TI EQ 20 S BMMI(CTYP) S " " "
41      IF TI EQ 21 S BMMI(CTYP) S " " / "
42      W = W + 1 S
43      ELSE S
44      IF DMTDY(EMS) EQ "C" S " CONSTANT "
45      THEN S
46      W = W + 1 S
47      IF DMTDY(EMS) S
48      TC = DMTDY(EMS) S
49      TC = ACVAL(CTIS) S
50      DSHN(1,TC,0,14) S
51      CTYP = 1 S " INTEGER "
52      ELSE S
53      IF DMTDY(EMS) EQ SLASH S " CHAR STRING "
54      THEN S
55      W = W + 1 S
56      TT = DMTDY(EMS) S
57      TC = ACVAL(CTIS) S
58      DSHN(1,TK,0,8) S
59      TC = ANLEN(CTIS) S
60      DSHN(1,TC,0,8) S
61      DSHN(3,SLASH,0,8) S
62      CTYP = 6 S " STRING "
63      DIRECT S
64      .CNAME W.STAG
65      INC W.STAG ; STRING MODE
66      JOURNAL
67      ELSE S " COMPOI ITEM PRINTED "
68      TK = TTYP(CTIS) S
69      TL = TADD(CTIS) S
70      TM = TFA(CTIS) S
71      TN = TNR(CTIS) S
72      DSHN(TK,TL,TN) S
73      CTYP = TTYP(CTIS) S
74      END IF S
75      END IF S
76      W = W + 1 S
77      " INCREMENT POLISH COUNTED "
78      END DO S
79      DUPN(0,ATI,0,14) S " RESULT OF POLISH CONF "
80      IF TI EQ 0 S " IF TI = 1 PERFORM DESIRED TASK "
81      THEN S
82      IF INSRQ EQ 0 S
83      THEN S
84      EXEC PCV45 S
85      DTRF(SNS) = 18 " TAG NOT CHECKED FOR 11/45 "
86      ELSE S
87      END IF S
88      IF INSRQ EQ 1 S
89      THEN S
90      EXEC PCV45 S
91      WAIT S
92      ELSE S
93      END IF S
94      IF INSRQ EQ 2 S
95      THEN S
96      WAIT S
97      ELSE S
98      END IF S
99      IF INSRQ EQ 3 S
100      THEN S
101      WAIT S
102      ELSE S
103      END IF S

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101 TURN S
102 EXEC PCVL2 S
103 WAIT S
104 ELSE S
105
106
107 END IF S
108 IF DIDES(41MSRCS) EQ 0 S '' THEN INVALID ACCESS ''
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JOVIAL ISS	* HARRIS JOVIAL COMPILER	PAGE
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[illegible]

[illegible]

[illegible]

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JOVIAL ISS                                *   WAPR75 JOVIAL COMPILER
                                           ---VERSION -3A
                                           PAGE 10
DRDP      0,0,0,0,DATYP,0,0,R          177
DRDP      0,0,0,0,DRADR,0,0,I6         177
PRDP      0,0,0,0,DADR,0,0,R           177
PRDP      0,0,0,0,DADR,0,0,R           177
JSP       B4,M,PUSH                     177
DATYP:    .RYTF 0                       177
          .RYTF 0                       177
DRADR:    .WORD 0                       177
DADR:     .RYTF 0                       177
DADR:     .RYTF 0                       177
          RTS PC                        177
JOVIAL.                                  177
END PROGRAM $                           177

```


DATA BASE REFERENCE LISTING

SECRET	13	5
RECARD	0	0
ESCHO	14	0
SLISH	9	74
ATCHO	9	74
DINDX	0	75
WUTYP	0	566
WUTYP	0	576
WUTYP	0	577
WUTYP	0	601
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WUTYP	0	720
WUTYP	0	721
WUTYP		

COMPACT SPACE USED = 1133

Notes

A-32

SPIN OPT
SPINISH
TIME:-00:14:19

SJON COMPUTER SCVTB
DATE:-22-AUG-77
TIME:-00:29:27
SPIN DTP
PTP VIO-03A
#DDN, SRC/DN
#COMPOL, 001/DE
#COMPOL, 001<COMPOL, YSS
#PPN, SRC<HI:/FA
SF00

SPIN JRVTSI


```

JOVIAL ISS          * HARRIS JOVIAL COMPILER          PAGE 1
                      ---VERSION -3a
PROGRAM PCV45 S
''-----
'' PCVTP - PCV45 IS VERSION OF PCVTP TO RESIDE IN 11/45. IT IS THE
'' SAME AS PCV11 EXCEPT THAT IT DOES NOT CHECK THE TAG, IT ONLY
'' EXECUTES THE COMMAND AND RETURNS TO CXFC
''-----
T = 0 S
IF MVTYP EQ 1 S '' SIGNIFIES EVENT ''
THEN S
  IF MVTYP EQ 1 S
  THEN S
    '' DISPLAY NOT AVAILABLE PRESENTLY ''
  ELSE S
    IF MVTYP EQ 2 S WRTKW(QEVENT,R0) & 'PRINT ''
  END IF S
  '' IF MVTYP GP 2 THEN RETURN TO 11/45 ''
  ELSE S
    IF MVTYP EQ 2 S '' REPORT ''
    THEN S
      '' CODE TO HANDLE REPORT WILL GO HERE ''
    ELSE S
      END IF S
    END IF S
  END IF S
DIRECT S
NOTIFY #INP45
EXIT
JOVIAL
END PROGRAM S

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DATA BASE REFERENCE LISTING

WVTP	576	9	0	16
MSTYP	577	9	0	16
EVENT	6501	2	1	40
I	1	13	0	16

COMPOUND SPACE USED = 1093

0 ERRORS

A-36

SFINISH
TIME:-00:31:27

A-37

SJON CQSPTE PCVIP

DATE:-22-AUG-77

TIME:-00:32:58

SPIN DTP

DTP V10-03A

BRN,SKC/DF

*COMBOL.001/DF

*COMBOL.001COMBOL.ISS

*PPN,SPCCTI:/FA

SEND

*
SPIN JONTAL

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JOVIAL ISS
* HARRIS JOVIAL COMPILER
---VERSION -3A
PAGE 1

PROGRAM PCV11 S
-----
!! PCV11 - RECEIVES INPUT FROM THE 11/45 IN RESPONSE TO A QUERY
!! AND CHECKS TAG AND THEN EXECUTES THE COMMAND !!
!! NOW RECORD OR DATA IS IN COMPOOL WAITING TO BE OUTPUT !!
!! NEED TO CHECK TAG BEFORE OUTPUT !!
!! DETAG IS DIFFERENT FOR EVENT AND REPORT : MSTYP IS QUALIFIER !!
-----
I = 0 S
CALL DETAG S
IF DTBES (SIS) EQ 0 S THEN TAG NO GOOD !!
THEN S
  SECPR(SIS) = SECPR(SIS) + 1 S
  !! IF TOO MANY SECURITY VIOLATIONS - LOCK UP TERMINAL !!
  IF SECPR(SIS) GP ANSV S
    THEN S
    LPDY(SIS) = 2 S
    ELSE S
  END IF S
  !! IF TOO MANY, LDY IS SET2 - TERMINAL LOCKS !!
  ELSE S !! TAG IS OK !!
  IF MSTYP EQ 1 S !! SIGNIFIES EVENT !!
    THEN S
    IF MVTP EQ 1 S
      THEN S
      !! DISPLAY NOT AVAILABLE PRESENTLY !!
      ELSE S
      IF MVTP EQ 2 S WRTHW(EVENT,80) & 'PRINT '
    END IF S
    !! IF MVTP GR 2 THEN RETURN TO 11/45 !!
    ELSE S
    IF MSTYP EQ 2 S !! REPORT !!
      THEN S
      !! CODE TO HANDLE REPORT WILL GO HERE !!
      ELSE S
    END IF S
  END IF S
END IF S
DIRECT S
NOTIFY #INP45
EXIT
JOVIAL
END PROGRAM S

```

DATA BASE REFERENCE LISTING

S									
MTYP	576	0	0	0	0	0	0	0	0
MTYP	577	0	0	0	0	0	0	0	0
ANSV	524	0	0	0	0	0	0	0	0
LPDY	1653	0	0	0	0	0	0	0	0
DTRES	1661	0	0	0	0	0	0	0	0
SFCERR	1664	0	0	0	0	0	0	0	0
EVFNT	6501	2	1	1	0	0	0	0	0
I	1	13	0	0	0	0	0	0	0

COMPONO, SPACE USED = 1093

0 ERRORS

A-40

SPINISH
TIME:-00:35:37

A-41

4J04 COMPILF SCOW
DATE:-22-AUG-77
TIME:-00:43:07
SPIN PTP
PIP V10-03A
RPN.SPC/DE

#COMPOL.001/0F

#COMPOL.001COMPOL.ISS

RPN.SPCRTI/FA

SEND

SPIN .INITAL

```

JUVIAL ISS * HADDIS JUVIAL COMPILEF PAGE 1
PROGRAM ACCOM
-----
ACCOM = ACCESS CONTROL CENTER PH - ACCEPTS INPUT FROM THE
      DATA KEYBOARD IN ORDER TO SET UP ACCESS PRIORITIES FOR
      EACH LSI TERMINAL. THEN IT TURNS ON THE INPUT PROCESSORS
      FOR THE LSI'S AND FOR THE 11/45 AND STARTS THE SYSTEM
      CYCLING.
INPUTS:
      KBUF = KEYBOARD INPUT BUFFER
OUTPUTS:
      ACKT = ACCESS KEYWORD TABLE - 1 ENTRY/LSI TERMINAL
      RNTBL = RANDOM NUMBER TABLE FOR USE BY TAG/DETAC
-----
      I = 0 $
      AGIN.
      LAFAD (QTM,1) $
      WNTKW ( TM ,62) $ 'PROMPT INPUT'
      PFDKW (KBUF,ATT) $ 'READ TERMINAL NUMBER'
      IF TI GR 2 $
      THEN $
      LAFAD (QTM,4) $
      WNTKW ( TM ,24) $ 'ERROR ; PLEASE REENTER'
      GOTO A1 $
      ELSE $
      END IF $
      J = 0 $
      IF IKRUF(S0) EQ A1 $ J = 1 $ 'SET TABLE INDEX'
      IF IKRUF(S0) EQ A2 $ J = 2 $
      IF J EQ 0 $
      THEN $
      LAFAD (QTM,4) $
      WNTKW ( TM ,24) $ 'ERROR ; PLEASE REENTER'
      GOTO A1 $ 'ERROR ; PLEASE REENTER'
      ELSE $
      END IF $
      LAFAD (QTM,2) $
      WNTKW ( TM ,48) $ 'PROMPT INPUT'
      PFDKW (KBUF,ATT) $ 'READ PRIORITY NUMBER'
      IF TI GR 2 $
      THEN $
      LAFAD (QTM,4) $
      WNTKW ( TM ,24) $ 'ERROR ; PLEASE REENTER'
      GOTO A2 $
      ELSE $
      END IF $
      IF IKRUF(S0) GR 3 $
      THEN $
      LAFAD (QTM,4) $
      WNTKW ( TM ,24) $ 'ERROR ; PLEASE REENTER'
      GOTO A2 $
      ELSE $
      END IF $
      LAFAD (QTM,4) $
      WNTKW ( TM ,24) $ 'ERROR ; PLEASE REENTER'
      GOTO A2 $
      ELSE $
      END IF $
      CASE IKRUF(S0) $

```



```

01 0 $
02 ACT(S1S) = UAPC $ "UNCLASSIFIED ACCESS"
03 1 $
04 ACT(S1S) = CACC $ "CONFIDENTIAL ACCESS"
05 2 $
06 ACT(S2S) = SACC $ "SECRET ACCESS"
07 3 $
08 ACT(S3S) = TSACC $ "TOP SECRET ACCESS"
09 CASE $
10 TAPAD (APM,3) $
11 WPTKY (TW,12R) $ "PROCVOT FOR NEXT TERMINAL OR START"
12 PEDKX (GRUP,ATT) $ "READ INPUT"
13 IF TI TO 1 $ GOTO ACIN $ "ENTERED ANOTHER TERMINAL"
14 ELSE A -PCFIN- WAS ENTERED"
15 PERFORM SOME INITIALIZATION BEFORE STARTING SYSTEM"
16 THE TRANSLATION TABLE AND SPEED NUMBER ARE INITIALIZED"
17 IN THE COMPUML. NOW CREATE A 256 WORD RANDOM"
18 MINIMAFZ TARDE "
19 RNGIN (CENTRL) $
20 LNOW TURNON INPUT PROCESSORS IN LSI "
21 IF ACT(S1S) NO 0 $
22 THEN $
23 DIRECT $
24 TURNON #IPUS1
25 JNVTAL
26 ELSE $
27 END IF $
28 IF ACT(S2S) NO 0 $
29 THEN $
30 DIRECT $
31 TURNON #IPUS2
32 JNVTAL
33 ELSE $
34 END IF $
35 TURNON INPUT PROCESSOR FOR 11/45"
36 DIRECT $
37 TURNON #IPUS45
38 EXIT
39 WSTK = $5
40 .GLOC DMGTN
41 .GLOC RANDU
42 NOV P0,-(SP)
43 NOV P1,-(SP)
44 NOV #256,P0
45 LDF (WSTK)+,AC0
46 STCT AC0,-(WSTK)
47 TST (WSTK)+
48 NOV (WSTK)+,P1
49 NOV P5,-(SP)
50 JSR #5,RANDU
51 AR 25
52 .WORD II
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JUVIAL ISS                                     * HARPIS JUVIAL COMPILER PAGE 3
--VERSION -3A

2S:      .WORD T?                               ;
        .WORD X                                ;

        MOV Y,(R1)+                            ;PUT RANDOM NUMBER IN TABLE
        R0,15                                  ;256 TIMES
        MOV (SP)+,P5                           ;RESTORE MSTK
        MOV (SP)+,P1                          ; AND OTHER REG.
        MOV (SP),Q0                             ;
        RTS PC
I1:      .WORD 0
I2:      .WORD 0
X:       .WORD 0

LRFAD:   .CLOBL LRFAD

        LDIF (MSTK)+,AC0
        STCFI AC0,-(MSTK)
        MOV R0,-(SP)
        MOV P1,-(SP)
        TST (MSTK)+
        MOV (MSTK)+,R0
        LDIF (MSTK)+,AC0
        STCFI AC0,(MSTK)+
        TST (MSTK)+
        ANI R0
        MOV SPAT,R1
        ADD R0,R1
        MOV R0,R1,Q(MSTK)+
        MOV (SP)+,P1
        MOV (SP)+,R0
        RTS PC
BAT:     .WORD 0
        .WORD MSG1
        .WORD MSG2
        .WORD MSG3
        .WORD MSG4

; I/O OUTPUT BUFFERS ----
MSG1:    .ASCII / ACCESS CONTROL CENTER READY/
        .BYTE 12,15
        .ASCII / PLEASE ENTER TERMINAL NUMBER/
        .BYTE 12,15
        .EVEN
MSG2:    .ASCII / ENTER PRIORITY OF 0-3 FOR DESIGNATED TERMINAL/
        .BYTE 12,15
        .EVEN
MSG3:    .ASCII / IF ALL TERMINALS HAVE BEEN ENTERED/
        .BYTE 12,15
        .ASCII / ENTER 'BEGIN' TO EXAMINE QUERY PROCESSING/
        .BYTE 12,15
        .ASCII / ELSE PRESS 'RETURN' TO ENTER ANOTHER TERMINAL/
        .BYTE 12,15
        .EVEN
MSG4:    .ASCII / ERROR: PLEASE REENTER/

```

JOVIAL ISS

DATE 12.15

FROM

JOVIAL

END PROGRAM S

HARRIS JOVIAL COMPILER
---VERSION -3A

PAGE 4

AS
AS
AS
AS

A-45

DATA BASE REFERENCE LISTING

S	5	13	0	0
A1	67	14	0	0
A2	70	14	0	0
TT	604	9	0	16
TM	611	9	0	16
UACC	625	9	0	16
SACC	626	9	0	16
CACC	627	9	0	16
TSACC	630	9	0	16
PNTBL	1200	2	1	256
KRIUF	1600	2	1	40
IKRIUF	1600	14	0	0
ACFT	1650	9	0	16
J	2	13	0	16

COMPPOOL SPACE USED = 1090

0 ERRORS

A-47

SPINISH
TIME:00:47:48

A-48

SJNR CONDITE IPJST
DATE:-22-AUG-77
TIME:-00:51:46

SRUN PIP
PIP V10-03A
RPN.SRC/DF

*COMPOL.001/DE

*COMPOL.001<COMPOL.ISS

*RPN.SPCCRT:/FA

SEND

*

SRUN J0VTAL


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DATA BASE REFERENCE LISTING

S	5	13	0	0
TI	604	9	0	16
GD	623	9	0	16
LADY	1453	9	0	16
RYTEC	1456	9	0	16
CRUF	1667	9	0	16
I	1	13	0	16
J	2	13	0	16
K	3	13	0	16
L	4	13	0	16

COMPOOL SPACE USED = 1093

0 ERRORS

A-51

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SRIN OPT
SFTHSH
TIME:-00:54:28
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A-52

SJOB CONTL COMPILE
DATE:-22-AUG-77
TIME:-00:57:07
SRUN PTP
PTP V10-03A
SRPN.SRC/OF

*COMPOL.001/DE

*COMPOL.001<COMPOL.ISS

SRPN.SRC<RT:/FA

SEOD

*

SRUN JOVIAL

JOVIAL ISS

PAGE 5

* HARPIS JOVIAL COMPILER
---VERSION -3A

PAGE 1

A-53

```

JOVIAL ISS          *  HARRIS JOVIAL COMPIER          PAGE 2
                      ---VERSION -3A
CCNTL SUBROUTINE $
''-----
'' COMMAND PARSING CONTROL - THIS ROUTINE CALLS THE PROPER ROUTINES ''
'' TO TRANSLATE AND EXECUTE A COMMAND LINE. ''
'' INPUTS ARE: ''
'' ICARD = TABLE CONTAINING THE COMMAND LINE ''
'' ICOL = POINTER TO ICARD ''
'' NCHRP = NUMBER OF CHARACTERS IN ICARD ''
'' OUTPUTS ARE: ''
'' EXECUTION OF THE COMMAND, SETS FLAG PRDY TO SIGNAL IT IS ''
'' READY FOR A NEW COMMAND. ''
''-----
'' INITIALIZE TABLES AND POINTERS ''
OPNDX = 0 $
PTNDX = 0 $
J = 0 $
DO UNTIL J EQ 40 $
  DCPTR(SJS) = 0 $
  J = J + 1 $
END DO $
J = 0 $
DO UNTIL J EQ 80 $
  DENTRY(SJS) = 0 $
  J = J + 1 $
END DO $
ICOL = 0 $
'' BEGIN LINE SCAN ''
DO UNTIL ICOL EQ NCHRP $
  IF ICARD(SICOL) NO IR $ GOTO ARAND $
  NBLNK $
  '' NBLNK SEARCHES FOR THE FIRST NON-BLANK CHARACTER ''
  DO UNTIL ICARD(SICOL) NO IR $
    ICOL = ICOL + 1 $
  END DO $
  BLNK $
  '' BLNK SEARCHES FOR THE FIRST BLANK CHARACTER ''
  '' DOESN'T CHANGE ICOL, STORES COLUMN IN RPTR ''
  RPTR = ICOL $
  DO UNTIL ICARD(SRPTR) EQ IR $
    RPTR = RPTR + 1 $
  END DO $
  ISLEN = RPTR - ICOL $
  CALL KSCAN $
  IF ICTYP EQ 0 $ '' MEANS NOT A KEYWORD ''
    THEN $
    CALL TTGEN $ '' SEE IF COMPOOL ITEM ''
    IF TTERR EQ 0 $ '' MEANS NOT A COMPOOL ITEM ''
    THEN $
    CALL CCON $ '' CHECK IF DECIMAL CONSTANT ''
    IF DCR EQ 0 $ '' MEANS NOT DECIMAL CONSTANTS ''
    THEN $
    DCOL(STTPTR) = ICOL $
    DLEN(STTPTR) = ISLEN $
    DCPTR = TTPIR $
  END DO $
  ARAND.

```



```

JOVIAL JSS                                * HARRIS JOVIAL COMPIER          PAGE 3
--VERSION -3A
TTDTR = TTDTR + 1 S
INTYP = 4 S '' DENOTES CHAR STRING DATA ''
CALL POLGN S
ICOL = ICOL + ISLEN S
IF S S
INTYP = 2 S '' DENOTES DECIMAL CONSTANT ''
CALL POLGN S
ICOL = ICOL + ISLEN S
END IF S
ELSE S
INTYP = 0 S '' COMPOUL ITEM ''
CALL POLGN S
ICOL = ICOL + ISLEN S
END IF S
ELSE S
IF TRNM EQ 23 S      MSTYP = 1 S '' EVENT ''
IF TRNM EQ 24 S      MSTYP = 2 S '' REPORT ''
IF TRNM EQ 1 S        MSTYP = 1 S '' DISPLAY ''
IF TRNM EQ 2 S        MSTYP = 2 S '' PRINT ''
IF TRNM EQ 3 S        MSTYP = 3 S '' DELETE ''
IF TRNM EQ 4 S        MSTYP = 4 S '' ADD ''
IF TRNM EQ 5 S        MSTYP = 5 S '' CHANGE ''
THEN S
IF TRNM IS 23 S
THEN S
INTYP = 1 S '' KEYWORD ''
CALL POLGN S
ELSE S
END IF S
ELSE S
END IF S
ICOL = ICOL + ISLEN S
END IF S
INTYP = 3 S '' SIGNAL END OF INPUT TO POLSHEN ''
CALL POLGN S
CALL CCYC S
PROV = 0 '' SIGNAL READY FOR NEXT COMMAND ''
LDDY(SINRCS) = 0 S '' SIGNAL INPUT PROCESSOR TO RESUME ''
DIRECT S
EXIT
JOVIAL
END SUBROUTINE S
END PROGRAM S

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DATA BASE REFERENCE LISTING

S	5	13	0	0	0
TCARD	0	14	0	0	0
IR	50	14	0	0	0
ICOL	106	0	0	0	0
ISLEN	563	0	0	0	0
OPHIX	564	9	0	0	0
ICTYP	565	9	0	0	0
PINDX	566	0	0	0	0
TRYEW	567	0	0	0	0
TTPTP	570	9	0	0	0
INTYP	571	0	0	0	0
PROY	572	9	0	0	0
DCR	573	0	0	0	0
DCOTD	575	9	0	0	0
WVJYP	576	0	0	0	0
WSTYP	577	0	0	0	0
NOCHR	600	9	0	0	0
TTEPR	620	0	0	0	0
APTR	621	9	0	0	0
INSPC	622	9	0	0	0
OPPTP	670	14	0	0	0
PHTRY	740	14	0	0	0
DCOL	1060	0	0	0	0
OLEN	1060	9	0	0	0
LRDY	1653	9	0	0	0
J	2	13	0	0	0

COMPONL SPACE USED = 1103

0 ERRORS

A-57

SPUN OPT

F0R0001010 UNABLE TO OPEN FILE

NAME SEQ

MAIN. 00000

A-58

SPIN MACRO
MACRO V06-04A
#CCNTI,,LP:KSYSYM,RPNWL,MOSMI,PPN,CND,USEND

A-59

SPICE
TIME-11:11:14

A-60

SJ0A
DATE:-17-AUG-77
TIME:-00:46:32
SRIN PTD
PTD V10-01A
WRITW.SRC/DE
S257 000002
DFO: WRITW.SRC
#DFO:WRITW.SRC<RI:/FA
SEND

SRIN MACRO
MACRO V06-04A
WRITW,LPICSYFV,WRITW.SRC

A-61

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO VOA-04A 17-AUG-77 00:46
TABLE OF CONTENTS

1- 2 SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:46 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SRTTU SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSDS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:46 PAGE 4
 SYSDS MULTIPROCESSOR OPERATING SYSTEM

```

1 000005 : SUBROUTINE TO WRITE KEYBOARD AND WAIT (TASK SW)
2      WSTK = $5
3      .GLOBAL WPTKW
4 000000 WPTKW:
5 000000 172425 LDF (WSTK)+,AC0 : CONVERT TO FIXED
6 000002 172445 STCFI AC0,-(WSTK) :
7 000004 005725 TST (WSTK)+ : PUT BYTE COUNT IN DEVA
8 000006 012567 MOV (WSTK)+,BCK : CONVERT TO FIXED
9 000012 172425 LDF (WSTK)+,AC0 :
10 00014 175445 STCFI AC0,-(WSTK) :
11 00016 005725 TST (WSTK)+ :
12 00020 010046 MOV R0,-(SP)
13 00022 010146 MOV R1,-(SP)
14 00024 010246 MOV R2,-(SP)
15 00026 012500 MOV (WSTK)+,R0 : GET BUFFER ADDRESS
16 00030 012702 MOV $1AUF,R2
17 00034 014701 MOV RCK,R1
18 00040 000134 1S:
19 00040 112022 MOV R (R0)+,(R2)+ : MOVE DATA TO LOCAL BUFFER
20 00042 077102 SDR R1,16 : MAX OF 80 CHAR. LINE
21 00044 014701 MOV RCK,R1
22 00050 022701 CVP $70,,R1
23 00054 003410 RIF 25 : INSERT LF
24 00056 112722 MOV R $12,(R2)+ : INSERT CR
25 00062 112722 MOV R $15,(R2)+ : CHANGE BYTE COUNT
26 00064 052767 ADD $2,RCK
27 00074 000213 RD 35
28 00076 142701 SDR $70,,R1
29 00102 005201 TNC R1
30 00104 140107 SDR R1,R2
31 00106 112722 MOV R $12,(R2)+ : INSERT LF
32 00112 112722 MOV R $15,(R2)+ : INSERT CR
33 00116 012767 MOV $R0,,RCK : CHANGE BYTE COUNT
34 00124 000050 3S:
35 00124 000124 TESTIO DEVRK,FOBK,3S : TEST I/O
36 00134 000134 STOPIO DEVRK,FOBK : WRITE TO DISK
37 00142 000142 WAITIO DEVRK,ERRK : WAIT (TASKSW)
38 00150 000150 FGBK:
39 00150 012402 MOV (SP)+,R2 : RESTORE REGISTERS
40 00152 012401 MOV (SP)+,R1
41 00154 012400 MOV (SP)+,R0
42 00156 000207 RTS PC
43 00160 000001 DEVRK: .WORD 1 : FORWARD LINK

```


SYSDPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:46 PAGE 4-1
 SYSDPS MULTIPROCESSOR OPERATING SYSTEM

44 00162 000000	.WORD	0	:PM #, PAGE
45 00164 000000	.WORD	0	:DEV, UNIT
46 00166 000000	.WORD	0	:STATUS
47 00170 000002	.WORD	2	:FUNCTION
48 00172 000200	.WORD	LAUF	:R RUF
49 00174 000000	.WORD	0	:BYTE COUNT
50 00176 000000	.WORD	0	:DDF
51 00200	.R1KW	40.	:LOCAL RUF.
52	.END		

SYSDS (MULTIPROCESSOR SYSTEM) MACHO V06-04A 17-AUG-77 00:46 PAGE 4-2
SYMBOL TABLE

AC0	=000000	AC1	=0000001	AC2	=0000002
AC3	=0000003	AC4	=0000004	AC5	=0000005
ACK	0001749	P0	= 000001	P1	= 000002
R10	= 002000	R11	= 004000	R12	= 010000
R13	= 020000	R14	= 040000	R15	= 100000
R2	= 000004	R3	= 000010	R4	= 000020
R5	= 000040	R6	= 000100	R7	= 000200
R8	= 000400	R9	= 001000	CP	= 000005
DEVER	0001609	OK	= 000001	D.PCATE	000014
D.HIPE	000017	D.DOF	= 000016	D.DEV	= 000004
D.FL	= 000000	D.FUNC	000010	D.PACE	000003
D.DM	= 000002	D.STATE	000006	D.WHTE	000005
FRPK	0001509	EXIT	= 104411	T.ENDPE	000006
I.FL	= 000000	I.TIME	000002	I.TVLF	000004
KP	= 000000	LAUF	000200R	LP	= 000004
MSTK	=0000005	WT	= 000002	M.DSA	= 000006
M.FLG	= 000003	M.FWA	= 000004	M.TPTE	000014
M.TCRW	000016	M.LGT	= 000010	M.NM1	= 000022
M.NM2	000024	M.DT	= 000012	M.DM	= 000026
M.DDCE	000027	M.BIN	= 000001	M.SUSE	000002
M.WSTE	000000	M.WDT	= 000020	PAGE.0E	000000
PAGE.1E	000001	PAGE.2E	000002	PAGE.3E	000003
PAGE.4E	000004	PAGE.5E	000005	PAGE.6E	000006
PR	= 177000	DT	= 000006	P.LCN	= 000032
P.AC1	= 000042	P.AC2	= 000052	P.AC3	= 000062
P.AC4	= 000072	P.AC5	= 000102	P.PFC	= 000002
P.FLG	= 000026	P.FPS	= 000030	P.PC	= 000020
P.PGF	= 000024	P.DSW	= 000022	P.DN	= 000004
P.D1	= 000006	P.D2	= 000010	P.D3	= 000012
P.D4	= 000014	P.D5	= 000016	R6	=0000006
P7	=0000007	SRP	= 177570	TASKSW	104410
TEPW	= 104412	TM	= 000003	WAITE	= 104404
WATW	000000G	.TPAP	= 104400		
.AHS.	000000				
	000320				

ERRORS DETECTED: 0
FREE CORE: 14073. WORDS
WRTW,LPICSYSW,WRTKW,SPC

FREE CORE: 14073. WORDS

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SFINISH
TIME:-00:47:34

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:48
TABLE OF CONTENTS

1- 2 SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSMPS (MULTIPROCESSOR SYSTEM) MACPD V06-04A 17-AUG-77 00:48 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SRCTL SYSMPS MULTIPROCESSOR OPERATING SYSTEM

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SYNOPS (MULTIPROCESSOR SYSTEM; VACON V06-04A 17-AUG-77 00:48 PAGE 4
SYNOPS MULTIPROCESSOR OPERATING SYSTEM

```

1 000005      : SUBROUTINE TO WRITE KEYBOARD AND NO WAIT (TASK SW)
2      WSTK = 85
3      .GLOBAL WSTK
4 000000      WRTK:
5 000000      LDF (WSTK)+,AC0
6 000002      STCF AC0,-(WSTK)
7 000004      TST (WSTK)+
8 000006      MOV (WSTK)+,RCK
9 000012      LDF (WSTK)+,AC0
10 000014      STCF AC0,-(WSTK)
11 000016      TST (WSTK)+
12 000020      MOV R0,-(SP)
13 000022      MOV R1,-(SP)
14 000024      MOV R2,-(SP)
15 000026      MOV (WSTK)+,P0
16 000030      MOV $LBUF,R2
17 000034      MOV RCK,R1
18 000040      MOV (R0)+,(R2)+
19 000042      MOV R1,$
20 000044      MOV RCK,R1
21 000046      CMP #79,,R1
22 000050      RLE
23 000054      MOV R12,(R2)+
24 000056      MOV R15,(R2)+
25 000062      ADD #2,RCK
26 000064      MOV R12,RCK
27 000074      MOV R15,R1
28 000076      MOV R12,R1
29 00102      MOV R12,(R2)+
30 00104      MOV R15,(R2)+
31 00106      MOV R12,RCK
32 00112      MOV R15,RCK
33 00114      MOV R12,RCK
34 00124      TESTN DEVAR,ERRK,35
35 00126      STRATN DEVAR,ERRK
36 00134      MOV (SP)+,R2
37 00142      MOV (SP)+,R1
38 00144      MOV (SP)+,P0
39 00146      PLS PC
40 00150      .WORD 1
41 00152      .WORD 0
42 00154      .WORD 0
43 00156      .WORD 0

```


SYSMDS (MULTIPROCESSOR SYSTEM) MICRO V06-04A 17-AUG-77 00:48 PAGE 4-1
 SYSMDS MULTIPROCESSOR OPERATING SYSTEM

44 00154 000000	.WDRD	0	:DEV. UNIT
45 00160 000000	.WDRD	0	:STATUS
46 00162 000002	.WDRD	2	:FUNCTION
47 00164 000172	.WDRD	LAUF	:B. PUPR
48 00166 000000 ACK:	.WDRD	0	:BYTE COUNT
49 00170 000000	.WDRD	0	:DUP
50 00172	.ALRW	40.	:LOCAL RUF.
51	000001		
			.END

SYSDS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:44 PAGE 4-2
SYMBOL TABLE

AC0	=000000	AC1	=000001	AC2	=000002
AC3	=000003	AC4	=000004	AC5	=000005
ACK	000166D	AD	= 000001	AD1	= 000002
AD0	= 000000	AD11	= 000000	AD12	= 000000
AD3	= 000000	AD14	= 000000	AD15	= 000000
AD2	= 000000	AD3	= 000001	AD4	= 000020
AD5	= 000040	AD6	= 000100	AD7	= 000200
AD8	= 000000	AD9	= 000100	ADP	= 000005
DEFVAR	000152R	ADK	= 000001	ADACTE	000014
D.HIPE	000012	ADDF	= 000016	ADDEV	= 000004
D.FL	= 000000	ADFINCE	000010	ADPACE	000003
D.PW	= 000000	ADSTATE	000006	ADUNITE	000005
ERR	000142R	EXIT	= 10441	T.ADDR	000006
I.FL	= 000000	T.TIME	= 000002	T.TYPE	000004
KR	= 000000	LAUF	000172D	LP	= 000004
MSTK	=000005	WT	= 000002	W.DSA	= 000006
M.FLG	= 000003	W.FWA	= 000004	W.TCHT	000014
M.TCRW	000016	W.LGT	000010	W.HM1	= 000022
M.NM2	000024	W.DPT	= 000012	W.DW	= 000026
M.PDCE	000027	W.DIN	= 000001	W.SUSP	000002
M.WAIT	000000	W.WOT	= 000020	PAGE.0	= 000000
PAGE.1	= 000001	PAGE.2	= 000002	PAGE.3	= 000003
PAGE.4	= 000004	PAGE.5	= 000005	PAGE.6	= 000006
PR	= 177000	PT	= 000006	P.ACO	= 000032
P.AC1	= 000042	P.AC2	= 000052	P.AC3	= 000042
P.AC4	= 000072	P.AC5	= 000102	P.PEG	= 000002
P.FLG	= 000026	P.PDS	= 000030	P.PC	= 000020
P.PGE	= 000024	P.PSW	= 000022	P.P0	= 000004
P.P1	= 000006	P.P2	= 000010	P.P3	= 000012
P.P4	= 000014	P.P5	= 000016	P6	=000006
P7	=000007	SPR	= 177570	TASKSW	104410
TERM	= 104412	TW	= 000003	WAIT6	= 104404
WPTK	000000RG	.TRAP	= 104400		
.ABS.	000000				
	000312				
ERRORS DETECTED:	0				
FREE CODE:	13345.WPDS				
WRITK,LP:	<SYSDS,WRITK.SRC				

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SYSMPS (MULTIPROCESSOR SYSTEM) MACPC V06-04A 17-AUG-77 00:51
TABLE OF CONTENTS

1- 2 SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSMDS (MULTIPROCESSOR SYSTEM) MACRO V06-04 17-AUG-77 00:51 PAGE 1

1 .TITLE SYSMDS (MULTIPROCESSOR SYSTEM)
2 .SATTL SYSMDS MULTIPROCESSOR OPERATING SYSTEM

SYSDPS (MULTIPROCESSOR SYSTEM) MICRO V06-04A 17-AUG-77 00:51 PAGE 4
SYSDPS MULTIPROCESSOR OPERATING SYSTEM

```

1      : SUBROUTINE TO READ DISK, NO WAIT.
2      MSTK = $5
3      .GLOBAL DISK
4      000000
5      172425
6      000000 172425
7      000000 175435
8      000004 005725
9      000006 012567
10     000104
11     000012 172425
12     000014 175435
13     000016 005725
14     000020 012567
15     000076
16     000024 172425
17     000026 175435
18     000030 005725
19     000032 012567
20     000062
21     000036 005767
22     000042 000004
23     000044 000401
24     000046 000000
25     000050
26     000052 012767
27     000054 000001
28     177762
29     000064
30     000066 15
31     000074
32     00102
33     00104 000207
34     00106 000001
35     00110 000000
36     00112 000000
37     00114 000505
38     00116 000000
39     00120 000000
40     00122 000000
41     00124 000000
42     00126 000000
43     00130 000000
44     00132 000000
45     00134 000000
46     000001
47     .END

```

DISK:

LOF (MSTK)+,AC0 : CONVERT TO FIXED
STCFT AC0,-(MSTK)
TST (MSTK)+
MOV (MSTK)+,RUPRD

LOF (MSTK)+,AC0 : CONVERT TO FIXED
STCFT AC0,-(MSTK)
TST (MSTK)+
MOV (MSTK)+,SECT : ADDR OF SECTOR TO DEVB

LOF (MSTK)+,AC0 : CONVERT TO FIXED
STCFT AC0,-(MSTK)
TST (MSTK)+
MOV (MSTK)+,RCD : BYTE COUNT TO DEVB

TST ICHK
RNE TFRP
RR FRST
.WORD 0

TTTTO DEVRD,TFRP
MOV #1,ICLK

TESTO DEVRD,FRPD,15
STPTO DEVRD,FRPD

RTS PC
.WORD 1
.WORD 0
.BYTE 1,1

.WORD 0
.WORD 505
.WORD 0
.WORD 0
.WORD 0
.WORD 0,0,0,0,0

FORWARD LINK
FMS, PAGE
DEVICE, UNIT *

STATUS
FUNCTION - READ
RUPRD
BYTE COUNT
SECTOR ADDR.
RESERVED FOR DISK DRIVER.

SYSDS (MULTIPROCESSOR SYSTEM) MICRO V06-04A 17-AUG-77 00:51 PAGE 4-1
SYMBOL TABLE

AC0	=000000	AC1	=000001	AC2	=000002
AC3	=000003	AC4	=000004	AC5	=000005
RC0	000120R	R0	000116R	R1	=000001
R1	=000002	R10	=002000	R11	=004000
R12	=010000	R13	=020000	R14	=040000
R15	=100000	R2	=000004	R3	=000010
R4	=000020	R5	=000040	R6	=000100
R7	=000200	R8	=000400	R9	=001000
CR	=000005	CV0	=000104R	CTSKP	000000RG
OK	=000001	D.ACMT	000014	D.RUPP	000012
D.DDF	=000016	D.DFV	=000004	D.FL	=000000
D.FUNC	000010	D.PAGE	000003	D.PW	=000002
D.STATE	000004	D.UNITE	000005	EDD	000102P
EXIT	=104111	FIRST	000050R	ICPK	000046P
IFRR	000044R	I.ADDR	000004	I.FL	=000000
I.TTYP	000002	I.TYPE	000004	KR	=000000
IP	=000004	WTK	=000005	WT	=000002
W.DSI	=000004	W.FLG	=000003	W.FWA	=000004
W.ICRI	000014	W.ICRW	000016	W.IGT	=000010
W.NAMI	000022	W.NAM2	000024	W.OPT	=000012
W.DW	=000026	W.PPCC	000027	W.PUN	=000001
W.SUSD	000002	W.WATT	000000	W.WOT	=000020
PAGE.0	000000	PAGE.1	=000001	PAGE.2	=000002
PAGE.3	=000003	PAGE.4	=000004	PAGE.5	=000005
PAGE.6	000004	PP	=177000	PT	=000006
P.AC0	=000032	P.AC1	=000042	P.AC2	=000052
P.AC3	=000062	P.AC4	=000072	P.AC5	=000102
P.BEC	=000002	P.FLG	=000026	P.FPS	=000030
P.PC	=000020	P.PGE	=000024	P.PSW	=000022
P.R0	=000004	P.R1	=000006	P.P2	=000010
P.R3	=000012	P.R4	=000014	P.P5	=000016
P6	=000006	P7	=000007	SECT	=000122P
SWR	=177570	TASKSW	104410	TERM	=104412
TW	=000003	WAITS	=104404	.TRAP	=104400

. ABS. 000000 000
000134 001
ERRORS DETECTED: 0
PAGE CORP: 13373 WORDS
DISK, LPI<SYN, DISK, SEC

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SYSMPS (MULTIPROCESSOR SYSTEM) MICRO V06-044 17-AUG-77 00:53
TABLE OF CONTENTS

1- 2 SYSMPS MULTIPROCESSOR OPERATING SYSTEM

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SYSMDS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:53 PAGE 1

1 .TITLE SYSMDS (MULTIPROCESSOR SYSTEM)
2 .SRCTL SYSMDS MULTIPROCESSOR OPERATING SYSTEM

```

1  SUBROUTINE TO WRITE TO PRINTER AND NO WAIT
2  MSTK = 85
3  .GLOBAL PRINT
4  PRINT:
5  000005 000000
6  000000 172425
7  000000 175445
8  000000 005725
9  000000 012567
10 000202
11 000012 172425
12 000014 175445
13 000016 005725
14 000020 010045
15 000022 010145
16 000024 010245
17 000026 012500
18 000030 012702
19 000220
20 00034 016701
21 000154
22 00040
23 00042 112022
24 00044 177102
25 00046 016701
26 00048 000144
27 00050 022701
28 00052 000203
29 00054 003410
30 00056 112722
31 00058 000012
32 00060 112722
33 00062 000015
34 00064 062767
35 00066 000002
36 00068 000120
37 00070 000413
38 00072 162701
39 00074 000202
40 00076 005201
41 00078 162102
42 00080 00104
43 00082 112722
44 00084 000012
45 00086 112722
46 00088 000015
47 00090 000204
48 00092 000070
49 00094 005767
50 00096 000004
51 00098 001010
52 00100 000401
53 00102 000000
54 00104 000000
55 00106 000000
56 00108 000000
57 00110 000000
58 00112 000000
59 00114 000000
60 00116 000000
61 00118 000000
62 00120 000000
63 00122 000000
64 00124 000000
65 00126 000000
66 00128 000000
67 00130 000000
68 00132 000000
69 00134 000000
70 00136 000000
71 00138 000000
72 00140 000000
73 00142 000000
74 00144 000000
75 00146 000000
76 00148 000000
77 00150 000000
78 00152 000000
79 00154 000000
80 00156 000000
81 00158 000000
82 00160 000000
83 00162 000000
84 00164 000000
85 00166 000000
86 00168 000000
87 00170 000000
88 00172 000000
89 00174 000000
90 00176 000000
91 00178 000000
92 00180 000000
93 00182 000000
94 00184 000000
95 00186 000000
96 00188 000000
97 00190 000000
98 00192 000000
99 00194 000000
100 00196 000000
101 00198 000000
102 00200 000000
103 00202 000000
104 00204 000000
105 00206 000000
106 00208 000000
107 00210 000000
108 00212 000000
109 00214 000000
110 00216 000000
111 00218 000000
112 00220 000000
113 00222 000000
114 00224 000000
115 00226 000000
116 00228 000000
117 00230 000000
118 00232 000000
119 00234 000000
120 00236 000000
121 00238 000000
122 00240 000000
123 00242 000000
124 00244 000000
125 00246 000000
126 00248 000000
127 00250 000000
128 00252 000000
129 00254 000000
130 00256 000000
131 00258 000000
132 00260 000000
133 00262 000000
134 00264 000000
135 00266 000000
136 00268 000000
137 00270 000000
138 00272 000000
139 00274 000000
140 00276 000000
141 00278 000000
142 00280 000000
143 00282 000000
144 00284 000000
145 00286 000000
146 00288 000000
147 00290 000000
148 00292 000000
149 00294 000000
150 00296 000000
151 00298 000000
152 00300 000000
153 00302 000000
154 00304 000000
155 00306 000000
156 00308 000000
157 00310 000000
158 00312 000000
159 00314 000000
160 00316 000000
161 00318 000000
162 00320 000000
163 00322 000000
164 00324 000000
165 00326 000000
166 00328 000000
167 00330 000000
168 00332 000000
169 00334 000000
170 00336 000000
171 00338 000000
172 00340 000000
173 00342 000000
174 00344 000000
175 00346 000000
176 00348 000000
177 00350 000000
178 00352 000000
179 00354 000000
180 00356 000000
181 00358 000000
182 00360 000000
183 00362 000000
184 00364 000000
185 00366 000000
186 00368 000000
187 00370 000000
188 00372 000000
189 00374 000000
190 00376 000000
191 00378 000000
192 00380 000000
193 00382 000000
194 00384 000000
195 00386 000000
196 00388 000000
197 00390 000000
198 00392 000000
199 00394 000000
200 00396 000000
201 00398 000000
202 00400 000000
203 00402 000000
204 00404 000000
205 00406 000000
206 00408 000000
207 00410 000000
208 00412 000000
209 00414 000000
210 00416 000000
211 00418 000000
212 00420 000000
213 00422 000000
214 00424 000000
215 00426 000000
216 00428 000000
217 00430 000000
218 00432 000000
219 00434 000000
220 00436 000000
221 00438 000000
222 00440 000000
223 00442 000000
224 00444 000000
225 00446 000000
226 00448 000000
227 00450 000000
228 00452 000000
229 00454 000000
230 00456 000000
231 00458 000000
232 00460 000000
233 00462 000000
234 00464 000000
235 00466 000000
236 00468 000000
237 00470 000000
238 00472 000000
239 00474 000000
240 00476 000000
241 00478 000000
242 00480 000000
243 00482 000000
244 00484 000000
245 00486 000000
246 00488 000000
247 00490 000000
248 00492 000000
249 00494 000000
25
```


SYNOPS (MULTIPROCESSOR SYSTEM) MACRO V04-04A 17-AUG-77 00:53 PAGE 4-1
SYNOPS MULTIPROCESSOR OPERATING SYSTEM

```

177762
42 00152      TFRP:
43 00152      3S:
44 00152
45 00162
46 00170      FRFP:
47 00170 012602
48 00172 012601
49 00174 012600
50 00176 002007
51 00200 000001 DFVRP:
52 00202 000000
53 00204      004
54 00205      000
55 00206 000000
56 00210 000000
57 00212 0002201
58 00214 000000 RCPN:
59 00220 000000 PRUF:
60 000001

TESTIN DFVRP,FRFP,3S      ;TEST Y/O
STATIN DFVRP,FRFP        ;WRITE TO PRINTER

MOV      (SP)+,R2
MOV      (SP)+,R1
MOV      (SP)+,R0
RTS      PC
; PESTORE REGISTERS
; FORWARD LINK
; DW 5, PAGE
; DFV,UNIT
; STATUS
; FUNCTION
; B FUPR
; BYTE COUNT
; INDF
; LOCAL RUF.

```

SYSDPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:53 PAGE 4-2
SYMBOL TABLE

AC0	=000000	AC1	=000001	AC2	=000002
AC3	=000003	AC4	=000004	AC5	=000005
ACPN	000214P	AO	= 000001	AI	= 000002
AI0	= 000000	AI1	= 004000	AI2	= 010000
AI3	= 000000	AI4	= 000000	AI5	= 100000
A2	= 000004	A3	= 000010	A4	= 000020
A5	= 000020	A6	= 000100	A7	= 000200
A8	= 000200	A9	= 001000	CP	= 000005
DFVBP	000200P	OK	= 000001	O.PCHT	000014
D.BHSP	000017	O.DDF	= 000014	O.PEV	= 000004
D.FL	= 000000	O.FUNC	000010	O.PAGE	000003
D.BH	= 000002	O.STAT	000006	O.UNIT	000005
EBOP	000170P	EXIT	= 104111	POST	000134P
ICBK	000134P	TEPR	000152P	T.ADDP	000004
I.FL	= 000000	I.TTMD	000002	I.TYPE	000004
KA	= 000000	LP	= 000004	NETK	=000005
MT	= 000002	M.OSA	= 000006	M.FLG	= 000003
M.FWA	= 000004	M.ICATE	000014	M.TCPK	000016
M.LCT	= 000010	M.NMI	000022	M.NMW2	000024
M.OPT	= 000012	M.DV	= 000026	M.PFCC	000027
M.PUN	= 000001	M.SUSP	000002	M.WATT	000000
M.WOT	= 000020	DACE.O	= 000000	PAGE.1	= 000001
PAGE.2	= 000002	DACE.AE	000003	PAGE.4E	000004
PAGE.5	= 000005	DACE.K	000006	PRUF	000220P
PR	= 177000	PRINT	000000P	PT	= 000006
P.LCO	= 000032	P.AC1	= 000042	P.AC2	= 000052
P.LC3	= 000062	P.AC4	= 000072	P.AC5	= 000102
P.PEC	= 000002	P.FLG	= 000024	P.FPS	= 000030
P.PC	= 000020	P.PCF	= 000024	P.PSW	= 000022
P.S0	= 000004	P.B1	= 000006	P.P2	= 000010
P.P3	= 000012	P.B4	= 000014	P.P5	= 000016
R6	=000005	R7	=000007	SOP	= 177570
TASKSW	104410	TRPM	= 104412	TV	= 000003
WATTS	= 104404	.TRAP	= 104400		
.ABS.	000000				
	000424				
ERRORS DETECTED:	0				
FREE CORE:	13360. WORDS				
PRINT.LP:KSYN,PRINT.SPC					

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SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:54
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2 .SRATL SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSDPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:54 PAGE 4
 SYSDPS MULTIPROCESSOR OPERATING SYSTEM

```

1 000005      : SUBROUTINE TO READ A CARD AND NO WAIT
2      MSTK = 85
3      .GLOBL. REANC
4 000000      REANC:
5 000000 172425      LDF (MSTK)+,AC0      : CONVERT TO FIXED
6 000000 175445      STCFT AC0,-(MSTK)      :
7 000000 005725      TST (MSTK)+
8 000000 012567      MOV (MSTK)+,RUPRR      : ADDR OF BUFFER TO DEVR
9 000000 000072
10 000012 172425      LDF (MSTK)+,AC0      : CONVERT TO FIXED
11 000014 175445      STCFT AC0,-(MSTK)      :
12 000016 005725      TST (MSTK)+
13 000020 012567      MOV (MSTK)+,ACR      : BYTE COUNT TO DEVR
14 000022 000062
15 000024 005767      TST ICHK
16 000026 000004
17 000028 001010      RNF IERR
18 000030 000401      RD FPST
19 000032 000000      ICHK:
20 000034 000000      FPST:
21 000036 012767      INITIO DEVR,IERR
22 000038 000001      MOV #1,ICLK
23 000040 177762
24 000042      TFRP:
25 000044      15:
26 000046      DEVR,ERRR,15
27 000048      STATIO DEVR,ERRR
28 000050      RTS PC
29 000052      .WORD 1
30 000054      .WORD 0
31 000056      .BYTE 5,0
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737 001468      .WORD 0
738 001470      .WORD 0
739 001472      .WORD 0
740 001474      .WORD 0
741 001476      .WORD 0
742 001478      .WORD 0
743 001480      .WORD 0
744 001482      .WORD 0
745 001484      .WORD 0
746 001486      .WORD 0
747 001488      .WORD 0
748 001490      .WORD 0
749 001492      .WORD 0
750 001494      .WORD 0
751 001496      .WORD 0
752 001498      .WORD 0
753 001500      .WORD 0
754 001502      .WORD 0
755 001504      .WORD 0
756 001506      .WORD 0
757 001508      .WORD 0
758 001510      .WORD 0
759 001512      .WORD 0
76
```

AC0	=0000000	AC1	=0000001	AC2	=0000002
AC3	=0000003	AC4	=0000004	AC5	=0000005
ACR	000104R	ACR	000104R	AC	=0000001
R1	=0000002	R10	=0000010	R11	=0000011
R12	=0000012	R13	=0000013	R14	=0000014
R15	=0000015	R2	=0000002	R3	=0000003
R4	=0000004	R5	=0000005	R6	=0000006
R7	=0000007	R8	=0000008	R9	=0000009
CR	=0000000	DEVAR	0000000	CV	=0000001
D.PONTE	0000014	D.BUFF	0000012	D.DIF	=0000016
D.DEV	=0000004	D.FL	=0000000	D.FUNC	0000010
D.PAGE	0000003	D.DW	=0000002	D.STATE	0000006
D.UNITE	0000005	ERR	0000000	EXIT	=104411
FRST	0000014R	ICHR	0000034P	IFPP	0000052P
I.ADRB	0000006	I.FL	=0000000	I.TIME	0000002
I.TYPE	0000004	KA	=0000000	IP	=0000004
MSTK	=0000005	MT	=0000002	M.CSA	=0000006
M.FLG	=0000003	M.FVA	=0000004	M.TCPE	0000014
M.TCWE	0000016	M.LCT	=0000010	M.FM1	=0000022
M.NAV2	0000024	M.NPT	=0000012	M.SUSP	0000026
M.PONCE	0000027	M.RW	=0000001	M.SUSP	0000027
M.WATTE	0000000	M.WOT	=0000020	PAGE.0	=0000000
PAGE.1	0000001	PAGE.2	=0000002	PAGE.3	=0000003
PAGE.4	=0000004	PAGE.5	=0000005	PAGE.6	=0000006
PR	=170000	PT	=0000006	P.ACO	=0000032
P.AC1	=0000042	P.AC2	=0000052	P.AC3	=0000062
P.AC4	=0000072	P.ACS	=000102	P.PC	=0000002
P.FLG	=0000026	P.FDS	=0000030	P.PC	=0000020
P.PGE	=0000024	P.PSW	=0000022	P.P0	=0000004
P.R1	=0000004	P.P2	=0000010	P.P3	=0000012
P.P4	=0000014	P.P5	=0000016	PEINC	=000000RG
P6	=0000006	R7	=0000007	SWP	=177570
TASKSW	104410	TERM	=104412	TM	=0000003
WATS	=104404	.TRAP	=104400		
.ARS.	0000000				
	000112				

ERRORS DETECTED: 0
FREE CORP: 13345. WORDS
READC,CP:CSYSYM,PF30C,SR

SYSOPS (MULTIPROCESSOR SYSTEM) MACPO V0A-04A 17-AUG-77 00:55
TABLE OF CONTENTS

1- 2 SYSOPS MULTIPROCESSOR OPERATING SYSTEM

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SYSMPS (MULTIPROCESSOR SYSTEM) MAC00 V06-04A 17-AUG-77 00:55 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SRTTU SYSMPS MULTIPROCESSOR OPERATING SYSTEM

```

; SUBROUTINE TO WRITE TO DISK, NO WAIT.
      MCTV = 85
      .GLOBAL   DISKW
DISKW:
      LDF      (MSTK)*,ACD
      STCFI    ACD,-(MSTK)
      TST      (MSTK)+
      MOV      (MSTK)*,RUPRD
      .
      LDF      (MSTK)*,ACD
      STCFI    ACD,-(MSTK)
      TST      (MSTK)+
      MOV      (MSTK)*,SECT
      .
      LDF      (MSTK)*,ACD
      STCFI    ACD,-(MSTK)
      TST      (MSTK)+
      MOV      (MSTK)*,RCD
      .
      TST      ICHK
      RNE      FERR
      RP       FRST
      .WORD    0
      .
      JMTTIO   DRYRD,FERR
      MOV      $1,ICLK
      .
      TESTIO   DEVRD,FRRD,$1$
      STATTIO  DEVRD,FRRD
      .
      RTS      PC
      .WORD    1
      .WORD    0
      .BYTE    1,1
      .
      .WORD    0
      .WORD    $03
      .WORD    0
      .WORD    0
      .WORD    0
      .WORD    0
      .WORD    0,0,0,0,0
      .
      .END

```


AC0	=000000	AC1	=000001	AC2	=000002
AC3	=000003	AC4	=000004	AC5	=000005
ACD	000120R	RIERD	000116R	R0	=000001
R1	=000002	R10	=002000	P11	=004000
R12	=010000	R13	=000000	P14	=040000
R15	=100000	R2	=000004	P3	=000010
R4	=000020	R5	=000040	R6	=000100
R7	=000200	R8	=000400	R9	=001000
CR	=000005	DEVDR	000104R	DISKW	000000RG
DK	=000011	D.ACNT	000014	D.RIIFR	000012
D.DOF	=000016	D.DEV	=000004	D.FI	=000000
D.FINCE	000010	D.DAGE	000003	D.DW	=000002
D.STATE	000006	D.UNIT	000005	FRPD	000102R
EXIT	=104411	FRST	000050R	ICFK	000046R
IFB	000040R	I.ADDR	000004	I.FI	=000000
I.THR	000002	I.TYPE	000004	KR	=000000
LP	=000004	MTK	=000005	MT	=000002
M.DSA	=000006	M.FLG	=000003	M.FVA	=000004
M.ICRT	000014	M.ICRW	000016	M.IGT	=000010
M.NAM1	000022	M.NAM2	000024	M.OPI	=000012
M.PM	=000026	M.DPDC	000027	M.RUN	=000001
M.SUSP	000002	M.WAIT	000000	M.WDT	=000020
PAGE.0	=000000	PAGE.1	000001	PAGE.2	=000002
PAGE.3	=000003	PAGE.4	=000004	PAGE.5	=000006
PAGE.6	=000004	P4	=177000	PT	=000006
P.ACO	=000032	P.AC1	=000042	P.AC2	=000052
P.AC3	=000062	P.AC4	=000072	P.AC5	=000102
P.REG	=000002	P.FLG	=000026	P.FPS	=000030
P.PC	=000020	P.PGE	=000024	P.PSW	=000022
P.R0	=000004	P.R1	=000006	P.P2	=000010
P.R3	=000012	P.R4	=000014	P.P5	=000016
R6	=000006	R7	=000007	SFCT	=000122R
SWP	=177570	TASKSW	=104410	TEMP	=104412
TW	=000003	WATS	=104404	.TRAP	=104400

.ARS. 000000 000
000136 001
ERRORS DETECTED: 0
FREE CODE: 13373. WORDS
DISKW.LP:KSYW,DISKW.SRC

SYSPDS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:56
TABLE OF CONTENTS

1- 2 SYSPDS MULTIPROCESSOR OPERATING SYSTEM

0
SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:56 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SATTI. SYSMPS MULTIPROCESSOR OPERATING SYSTEM

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SYSMPS (MULTIPROCESSOR SYSTEM) MACPO V06-04A 17-AUG-77 00:56
TABLE OF CONTENTS

1- 2 SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:58 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SRTTU SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSDPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:58 PAGE 4
SYSDPS MULTIPROCESSOR OPERATING SYSTEM

```

1 000005      : SUBROUTINE TO WRITE TO PRINTER AND WAIT
2 000005      MSTR = 85
3 000005      .GLORU  PNTW
4 000000      PRNTW:
5 000000      LDF  (MSTR)+,AC0      : CONVERT TO FIXED
6 000000      STCFI AC0,-(MSTRK)      ;
7 000000      TST  (MSTRK)+
8 000000      MOV  (MSTRK)+,BCP      : PUT BYTE COUNT IN DEVP
9 000000      LDF  (MSTRK)+,AC0      : CONVERT TO FIXED
10 000000      STCFI AC0,-(MSTRK)      ;
11 000000      TST  (MSTRK)+
12 000000      MOV  R0,-(SP)
13 000000      MOV  R1,-(SP)
14 000000      MOV  R2,-(SP)
15 000000      MOV  (MSTRK)+,R0      : GET RUFFER ADDRESS
16 000000      MOV  #PRUF,R2
17 000000      MOV  RCP,R1
18 000000      1S:
19 000000      MOVA (R0)+,(R2)+      : MOVE DATA TO LOCAL RUFFER
20 000000      SDR  R1,1S
21 000000      MOV  BCP,R1      : MAX OF R0 CHAR. LINE
22 000000      CMP  #131,R1
23 000000      RLF  2S
24 000000      MOVA #12,(R2)+      : INSERT LF
25 000000      MOVA #15,(R2)+      : INSERT CR
26 000000      ADD  #2,BCP      : CHANGE BYTE COUNT
27 000000      BR  3S
28 000000      SUB  #130,R1
29 000000      JNC  R1
30 000000      SUB  R1,P2
31 000000      MOVA #12,(R2)+      : INSERT LF
32 000000      MOVA #15,(R2)+      : INSERT CR
33 000000      MOV  #132,BCP      : CHANGE BYTE COUNT
34 000000      3S:
35 000000      TST  ICHK
36 000000      RNF  IFRP
37 000000      RNF  FRST
38 000000      .WORD 0
39 000000      TCHK:
40 000000      FRST:
41 000000      INITI DEVRP,IFRP
42 000000      MOV  #1,ICLK
43 000000

```


SYSDS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 0015R PAGE 4-1
 SYSDS MULTIPROCESSOR OPERATING SYSTEM

```

17742
42 00152      TERR:
43 00152      38:
44 00152
45 00162      TESTIO DEVRP,FRPP,38
46 00170      STATIO DEVRP,FRPP
47 00176      WAITIO DEVRP,FRPP
48 00176      (SP)+,R2
49 00200      MOV      (SP)+,R1
50 00202      MOV      (SP)+,R0
51 00204      RTS      PC
52 00206      DEVRP:
53 00210      .WORD    1
54 00212      .BYTE    4,0
55 00214      .WORD    0
56 00216      .WORD    0
57 00220      .WORD    PRUF
58 00222      .WORD    0
59 00224      .WORD    0
60 00226      .RLKW    66.
61          .END

      : RESTORE REGISTERS
      : FORWARD LINK
      : DM #, PAGE
      : DEV,UNIT
      : STATUS
      : FUNCTION
      :A BUFP
      :BYTE COUNT
      :DCF
      :LOCAL BUF.

```

SYNOPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 00:58 PAGE 4-2
SYMBOL TABLE

AC0 = 0000000	AC1 = 0000001	AC2 = 0000002
AC3 = 0000003	AC4 = 0000004	AC5 = 0000005
ACP = 000222R	R0 = 0000001	P1 = 0000002
R10 = 0020000	R11 = 0040000	P12 = 0100000
R13 = 0200000	R14 = 0400000	R15 = 1000000
R2 = 0000004	R3 = 0000010	R4 = 0000020
R5 = 0000040	R6 = 0001000	P7 = 0002000
R8 = 0004000	R9 = 0010000	CP = 0000005
DEVRP = 000206R	DK = 0000001	D.PCHT = 000014
D.RUFRE = 000012	D.DDF = 000016	D.DFV = 000004
D.FL = 0000000	D.FUNC = 000010	D.PAGE = 000003
D.PM = 0000002	D.STATE = 000006	D.UNIT = 000005
ERPD = 000174R	EXIT = 104411	FEST = 000135R
YCHK = 000134R	TERP = 000152R	T.ADDR = 000004
T.FL = 0000000	T.TWR = 000002	T.TYPE = 000004
KR = 0000000	LD = 0000004	HSTK = 0000005
MT = 0000002	M.DSA = 000006	M.FLG = 000003
M.FPA = 0000004	M.ICRT = 000014	M.JCRV = 000016
M.LGT = 000010	M.NAW1 = 000022	M.NAW2 = 000024
M.NPI = 000012	M.PM = 000026	M.PROC = 000027
M.RIN = 000001	M.SUSP = 000002	M.VAIT = 000000
M.WDT = 000020	PAGE.0 = 000000	PAGE.1 = 000001
PAGE.2 = 000002	PAGE.3 = 000003	PAGE.4 = 000004
PAGE.5 = 000005	PAGE.6 = 000006	PRIF = 000226R
PP = 177000	PRNTW = 0000007G	PT = 000006
P.AC0 = 000032	P.AC1 = 000042	P.AC2 = 000052
P.AC3 = 000062	P.AC4 = 000072	P.AC5 = 000102
P.BEC = 000002	P.FLG = 000026	P.FPS = 000030
P.PC = 000020	P.PGE = 000024	P.PSM = 000022
P.R0 = 000004	P.R1 = 000006	P.R2 = 000010
P.R3 = 000012	P.R4 = 000014	P.R5 = 000016
P6 = 0000006	P7 = 000007	SWP = 177570
TASKSW = 104410	TERM = 104412	TW = 000003
WATTS = 104404	.TRAP = 104400	
.ARS. 000000	000	
.ARS. 000432	001	
ERRORS DETECTED: 0		
FREE CODE: 13369. WORDS		
PRINTW,LD: <SYSYW,PRINTW.SRC		

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:05
TABLE OF CONTENTS

1- 2 SYSMPS MULTIPROCESSOR OPERATING SYSTEM

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:05 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SRCTL SYSMPS MULTIPROCESSOR OPERATING SYSTEM

LINE	ADDRESS	OPERATION	DATA	COMMENT
1	000005	SUBROUTINE TO READ DISK & WAIT.		
2	000006	MSK = 84		
3	000007	CLOCAL		
4	000008	DSKRW:		
5	000009	LDF	(MSK)*.ACD	: CONVERT TO FIXED
6	000010	STCFI	ACD, -(MSK)	:
7	000011	TST	(MSK)+	
8	000012	MOV	(MSK)*.RUPRD	: ADDR OF OUTPUT RUPRD TO DEVA
9	000013	LDF	(MSK)*.ACD	: CONVERT TO FIXED
10	000014	STCFI	ACD, -(MSK)	:
11	000015	TST	(MSK)+	
12	000016	MOV	(MSK)*.SECT	: ADDR OF SECTOR TO DEVA
13	000017	LDF	(MSK)*.ACD	: CONVERT TO FIXED
14	000018	STCFI	ACD, -(MSK)	:
15	000019	TST	(MSK)+	
16	000020	MOV	(MSK)*.ACD	: BYTE COUNT TO DEVA
17	000021	TST	ICNK	
18	000022	RNF	IFRR	
19	000023	RR	FPST	
20	000024	.WORD	0	
21	000025	INITIO	DEVAD, IERR	
22	000026	MOV	8J, ICNK	
23	000027	ICNK		
24	000028	TERR:		
25	000029	IS:	DEVAD, ERRD, 16	
26	000030		DEVAD, ERRD	
27	000031		WAITIO	: WRITE DISK TO RUPFR
28	000032	ERRD:		
29	000033	DEVAD:	PC	
30	000034		1	: FORWARD LINK
31	000035		0	: PAGE
32	000036		1, 1	: DEVICE, UNIT :
33	000037		0	: STATUS
34	000038		505	: FUNCTION - READ
35	000039	RUPRD:		: RUPFR
36	000040	ACD:	0	: BYTE COUNT
37	000041	SECT:	0	: SECTOR ADDR.
38	000042		0, 0, 0, 0, 0	: RESERVED FOR DISK DRIVER.
39	000043			
40	000044			
41	000045			
42	000046			
43	000047			
44	000048			
45	000049			
46	000050			
47	000051			
48	000052			
49	000053			
50	000054			
51	000055			
52	000056			
53	000057			
54	000058			
55	000059			
56	000060			
57	000061			
58	000062			
59	000063			
60	000064			
61	000065			
62	000066			
63	000067			
64	000068			
65	000069			
66	000070			
67	000071			
68	000072			
69	000073			
70	000074			
71	000075			
72	000076			
73	000077			
74	000078			
75	000079			
76	000080			
77	000081			
78	000082			
79	000083			
80	000084			
81	000085			
82	000086			
83	000087			
84	000088			
85	000089			
86	000090			
87	000091			
88	000092			
89	000093			

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:06 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SBTTL SYSMPS MULTIPROCESSOR OPERATING SYSTEM


```

SYMSPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:06 PAGE 4
SYMSPS MULTIPROCESSOR OPERATING SYSTEM

1 :-----
2 : THIS PROGRAM READS FROM THE LA36 KEYBOARD AND STORES THE INPUT DAT
3 : IN THE DESIGNATED BUFFER. THE CALL IS :
4 : PUSH ADDR OF INPUT BUFFER
5 : : PUSH ADDR OF ACTUAL BYTE COUNT (RETURNED)
6 : : R4, R5, R6, R7
7 :-----
8 : MSTR = #5
9 : GLRCL READK
10 00000
11 00000 172495
12 00002 175445 STCFI (MSTR)+,AC0 : CONVERT TO FIXED
13 00004 005725 TST (MSTR)+ :
14 00006 012567 MOV (MSTR)+,BUFRK : ADDRESS OF INPUT BUFFER TO DEVR
15 00012 172425 LDF (MSTR)+,AC0 : CONVERT TO FIXED
16 00014 175445 STCFI AC0,-(MSTR) :
17 00016 005725 TST (MSTR)+ :
18 00020 010446 MOV R4,-(SP) : SAVE R4
19 00022 012504 MOV (MSTR)+,R4 : PUT ADDR TO RETURN ACTUAL BC INTO R4
20 00024 1S: TESTIO DEVRBK,KEPR,IS : TEST I/O DRIVER FOR KR
21 00034 STARTIO DEVRBK,KEPR : BEGIN READ
22 00042
23 00042 016714 MOV DEVRBK+16,AP4 : PUT ACTUAL RC INTO DESIGNATED ADDR
24 00046 012604 MOV (SP)+,R4 : RESTORE R4
25 00050 000207 RTS PC :
26 00052 000001 DEVRBK: : FORWARD LINK
27 00054 000 : PW#,PAGE #
28 00055 000 : BYTE
29 00056 000 : DEV,UNIT #
30 00057 000 : STATUS
31 00060 000000 : FUNCTION
32 00062 000001 : @ RUPR
33 00064 000000 : RUPR
34 00066 000120 : BYTE COUNT
35 00068 000000 :
36 00070 000001 :
37 00072 000001 :
38 00074 000001 :
39 00076 000001 :
40 00078 000001 :
41 00080 000001 :
42 00082 000001 :
43 00084 000001 :
44 00086 000001 :
45 00088 000001 :
46 00090 000001 :
47 00092 000001 :
48 00094 000001 :
49 00096 000001 :
50 00098 000001 :
51 00100 000001 :
52 00102 000001 :
53 00104 000001 :
54 00106 000001 :
55 00108 000001 :
56 00110 000001 :
57 00112 000001 :
58 00114 000001 :
59 00116 000001 :
60 00118 000001 :
61 00120 000001 :
62 00122 000001 :
63 00124 000001 :
64 00126 000001 :
65 00128 000001 :
66 00130 000001 :
67 00132 000001 :
68 00134 000001 :
69 00136 000001 :
70 00138 000001 :
71 00140 000001 :
72 00142 000001 :
73 00144 000001 :
74 00146 000001 :
75 00148 000001 :
76 00150 000001 :
77 00152 000001 :
78 00154 000001 :
79 00156 000001 :
80 00158 000001 :
81 00160 000001 :
82 00162 000001 :
83 00164 000001 :
84 00166 000001 :
85 00168 000001 :
86 00170 000001 :
87 00172 000001 :
88 00174 000001 :
89 00176 000001 :
90 00178 000001 :
91 00180 000001 :
92 00182 000001 :
93 00184 000001 :
94 00186 000001 :
95 00188 000001 :
96 00190 000001 :
97 00192 000001 :
98 00194 000001 :
99 00196 000001 :
100 00198 000001 :
101 00200 000001 :
102 00202 000001 :
103 00204 000001 :
104 00206 000001 :
105 00208 000001 :
106 00210 000001 :
107 00212 000001 :
108 00214 000001 :
109 00216 000001 :
110 00218 000001 :
111 00220 000001 :
112 00222 000001 :
113 00224 000001 :
114 00226 000001 :
115 00228 000001 :
116 00230 000001 :
117 00232 000001 :
118 00234 000001 :
119 00236 000001 :
120 00238 000001 :
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122 00242 000001 :
123 00244 000001 :
124 00246 000001 :
125 00248 000001 :
126 00250 000001 :
127 00252 000001 :
128 00254 000001 :
129 00256 000001 :
130 00258 000001 :
131 00260 000001 :
132 00262 000001 :
133 00264 000001 :
134 00266 000001 :
135 00268 000001 :
136 00270 000001 :
137 00272 000001 :
138 00274 000001 :
139 00276 000001 :
140 00278 000001 :
141 00280 000001 :
142 00282 000001 :
143 00284 000001 :
144 00286 000001 :
145 00288 000001 :
146 00290 000001 :
147 00292 000001 :
148 00294 000001 :
149 00296 000001 :
150 00298 000001 :
151 00300 000001 :
152 00302 000001 :
153 00304 000001 :
154 00306 000001 :
155 00308 000001 :
156 00310 000001 :
157 00312 000001 :
158 00314 000001 :
159 00316 000001 :
160 00318 000001 :
161 00320 000001 :
162 00322 000001 :
163 00324 000001 :
164 00326 000001 :
165 00328 000001 :
166 00330 000001 :
167 00332 000001 :
168 00334 000001 :
169 00336 000001 :
170 00338 000001 :
171 00340 000001 :
172 00342 000001 :
173 00344 000001 :
174 00346 000001 :
175 00348 000001 :
176 00350 000001 :
177 00352 000001 :
178 00354 000001 :
179 00356 000001 :
180 00358 000001 :
181 00360 000001 :
182 00362 000001 :
183 00364 000001 :
184 00366 000001 :
185 00368 000001 :
186 00370 000001 :
187 00372 000001 :
188 00374 000001 :
189 00376 000001 :
190 00378 000001 :
191 00380 000001 :
192 00382 000001 :
193 00384 000001 :
194 00386 000001 :
195 00388 000001 :
196 00390 000001 :
197 00392 000001 :
198 00394 000001 :
199 00396 000001 :
200 00398 000001 :
201 00400 000001 :
202 00402 000001 :
203 00404 000001 :
204 00406 000001 :
205 00408 000001 :
206 00410 000001 :
207 00412 000001 :
208 00414 000001 :
209 00416 000001 :
210 00418 000001 :
211 00420 000001 :
212 00422 000001 :
213 00424 000001 :
214 00426 000001 :
215 00428 000001 :
216 00430 000001 :
217 00432 000001 :
218 00434 000001 :
219 00436 000001 :
220 00438 000001 :
221 00440 000001 :
222 00442 000001 :
223 00444 000001 :
224 00446 000001 :
225 00448 000001 :
226 00450 000001 :
227 00452 000001 :
228 00454 000001 :
229 00456 000001 :
230 00458 000001 :
231 00460 000001 :
232 00462 000001 :
233 00464 000001 :
234 00466 000001 :
235 00468 000001 :
236 00470 000001 :
237 00472 000001 :
238 00474 000001 :
239 00476 000001 :
240 00478 000001 :
241 00480 000001 :
242 00482 000001 :
243 00484 000001 :
244 00486 000001 :
245 00488 000001 :
246 00490 000001 :
247 00492 000001 :
248 00494 000001 :
249 00496 000001 :
250 00498 000001 :
251 00500 000001 :
252 00502 000001 :
253 00504 000001 :
254 00506 000001 :
255 00508 000001 :
256 00510 000001 :
257 00512 000001 :
258 00514 000001 :
259 00516 000001 :
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283 00564 000001 :
284 00566 000001 :
285 00568 000001 :
286 00570 000001 :
287 00572 000001 :
288 00574 000001 :
289 00576 000001 :
290 00578 000001 :
291 00580 000001 :
292 00582 000001 :
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295 00588 000001 :
296 00590 000001 :
297 00592 000001 :
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299 00596 000001 :
300 00598 000001 :
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330 00658 000001 :
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333 00664 000001 :
334 00666 000001 :
335 00668 000001 :
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339 00676 000001 :
340 00678 000001 :
341 00680 000001 :
342 00682 000001 :
343 00684 000001 :
344 00686 000001 :
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359 00716 000001 :
360 00718 000001 :
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363 00724 000001 :
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384 00766 000001 :
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390 00778 000001 :
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392 00782 000001 :
393 00784 000001 :
394 00786 000001 :
395 00788 000001 :
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405 00808 000001 :
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475 00948 000001 :
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481 00960 000001 :
482 00962 000001 :
483 00964 000001 :
484 00966 000001 :
485 00968 000001 :
486 00970 000001 :
487 00972 000001 :
488 00974 000001 :
489 00976 000001 :
490 00978 000001 :
491 00980 000001 :
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564 01126 000001 :
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679 01356 000001 :
680 01358 000001 :
681 01360 000001 :
682 01362 000001 :
683 01364 000
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AD-A054 508

HARRIS CORP MELBOURNE FLA ELECTRONIC SYSTEMS DIV
INTELLIGENCE SECURITY SUBSYSTEM.(U)
MAR 78 F ANDERS, W MALL, R MCGILL

F/G 9/2

F30602-76-C-0445

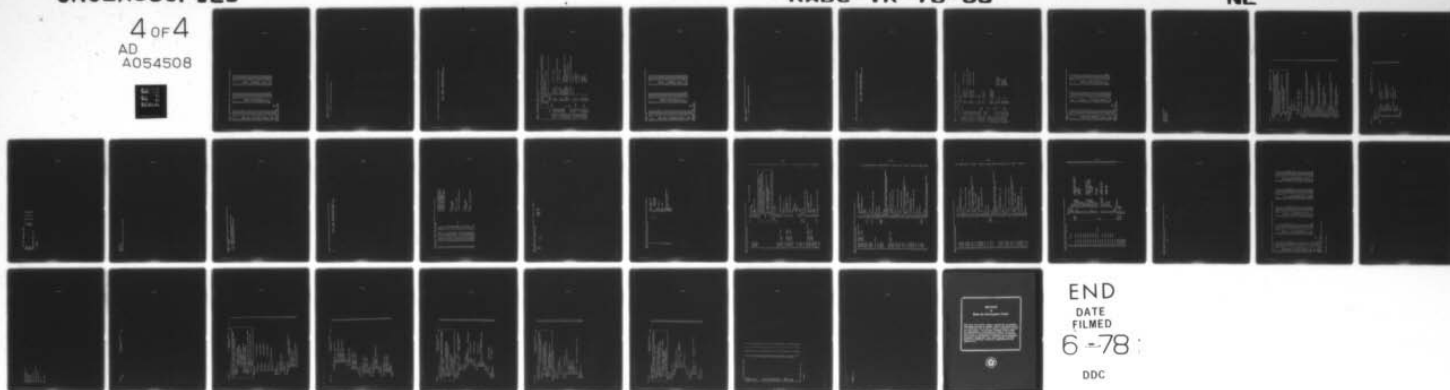
UNCLASSIFIED

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4 OF 4

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SYMSYS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:06 PAGE 4-1
SYMBOL TABLE

AC0 = 000000	AC1 = 0000001	AC2 = 0000002
AC3 = 0000003	AC4 = 0000004	AC5 = 0000005
RUFRK = 0000000	R0 = 0000001	R1 = 0000002
R10 = 0000000	R11 = 0000000	R12 = 0000000
R13 = 0000000	R14 = 0000000	R15 = 0000000
R2 = 0000000	R3 = 0000001	R4 = 0000002
R5 = 0000000	R6 = 0000000	R7 = 0000000
RR = 0000000	RQ = 0000000	CR = 0000005
DEVRK = 0000000	OK = 0000001	D.PCTE = 0000014
D.RUFR = 0000012	D.DNF = 0000014	D.DEV = 0000004
D.FL = 0000000	D.FUNC = 0000010	D.PACE = 0000003
D.PM = 0000002	D.STATE = 0000006	D.UNIT = 0000005
EXIT = 104411	I.ADDR = 0000005	I.FL = 0000000
I-TMR = 0000002	I.TYDF = 0000004	KR = 0000000
KERR = 0000002	LP = 0000004	MSTK = 0000005
MT = 0000002	M.DSA = 0000006	M.FLG = 0000003
M.FWA = 0000004	M.TCRTE = 0000014	M.ICRW = 0000016
M.LGT = 0000010	M.NAM1 = 0000022	M.NAM2 = 0000024
M.NDI = 0000012	M.PM = 0000026	M.PPDC = 0000027
M.RUN = 0000001	M.SUSP = 0000002	M.WAIT = 0000000
M.WDT = 0000020	PAGE.0 = 0000000	PAGE.1 = 0000001
PAGE.2 = 0000002	PAGE.3 = 0000003	PAGE.4 = 0000004
PAGE.5 = 0000005	PAGE.6 = 0000006	PP = 1770000
PI = 0000006	P.ACO = 0000037	P.AC1 = 0000047
P.AC2 = 0000052	P.AC3 = 0000062	P.AC4 = 0000072
P.AC5 = 0001002	P.REG = 0000002	P.FLG = 0000026
P.FPS = 0000030	P.PC = 0000020	P.PGF = 0000024
P.PSM = 0000072	P.R0 = 0000004	P.R1 = 0000006
P.R2 = 0000010	P.R3 = 0000012	P.R4 = 0000014
P.R5 = 0000014	READK = 0000000HG	R6 = 0000006
P7 = 0000007	TERM = 104412	TASKSW = 104410
TRAP = 104400	TM = 0000003	WAIT8 = 104404
ARS. 000000		
ARS. 000072		
ERRORS DETECTED: 0		
FREE CORE: 13401. WORDS		
READK,LP:CSYSYM,READK.SP		

SYSDPS (MULTIPROCESSOR SYSTEM) MACRO VO:0-04A 17-AUG-77 01:07
TABLE OF CONTENTS

1- 2 SYMPS MULTIPROCESSOR OPERATING SYSTEM

SYSMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:07 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SRITI SYSMPS MULTIPROCESSOR OPERATING SYSTEM

```

SYNOPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:07 PAGE 4
SYNOPS MULTIPROCESSOR OPERATING SYSTEM

1  :-----
2  : THIS PROGRAM READS FROM THE L336 KEYBOARD AND STORES THE INPUT DAT
3  : IN THE DESIGNATED BUFFER. THE CALL IS :
4  : PUSH ADDRESS OF INPUT BUFFER
5  : PUSH ADDRESS OF ACTUAL BYTE COUNT (RETURNED)
6  : .ISR R4,REDAK
7  :-----
8  :
9  : MSTR = %S
10 : .GLOBL REDAK
11 :
12 : REDAK:
13 : LDF (MSTR)+,AC0 ; CONVERT TO FIXED
14 : STCFI AC0,-(MSTR) ;
15 : TST (MSTR)+ ;
16 : MOV (MSTR)+,RUPRK ; ADDRESS OF INPUT BUFFER TO DEVR
17 :
18 : LDF (MSTR)+,AC0 ; CONVERT TO FIXED
19 : STCFI AC0,-(MSTR) ;
20 : TST (MSTR)+ ;
21 : MOV R4,-(SP) ; SAVE R4
22 : MOV (MSTR)+,R4 ; PUT ADDR TO RETURN ACTUAL PC INTO R4
23 : TESTIO DEVRPK,KEPR,18 ; TEST I/O DRIVER FOR KE
24 : STRIO DEVRPK,KEPR ; BEGIN READ
25 : WAITIO DEVRPK,KEPR ; WAIT FOR I/O TO COMPLETE
26 :
27 : MOV DEVRPK+16,SP4 ; PUT ACTUAL PC INTO DESIGNATED ADDR
28 :
29 : MOV (SP)+,R4 ; RESTORE R4
30 : RTS PC ; FORWARD LINK
31 : .WORD 1 ; DW#,PAGE #
32 : .BYTE 0,0 ;
33 : .BYTE 0,0 ; DEV,UNIT #
34 :
35 : .WORD 0 ; STATUS
36 : .WORD 1 ; FUNCTION
37 : .WORD 0 ; & RIIPR
38 : .WORD 80 ; BYTE COUNT
39 : .WORD 0 ; DDF
40 : .END

```


SYNOPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:07 PAGE 4-1
SYMBOL TABLE

AC0	=0000000	AC1	=0000001	AC2	=0000002
AC3	=0000003	AC4	=0000004	AC5	=0000005
BIFFW	000072R	R0	= 000001	R1	= 000002
R10	= 002000	R11	= 004000	R12	= 010000
R13	= 020000	R14	= 040000	R15	= 100000
R2	= 000004	R3	= 000010	R4	= 000020
R5	= 000040	R6	= 000100	R7	= 000200
R8	= 000400	R9	= 001000	C0	= 000005
DEVRM	000060R	RK	= 000001	R.BCMTE	000014
D.BIFFR	000012	D.DNF	= 000016	R.DSV	= 000004
D.FL	= 000000	D.FUNC	000010	D.PACF	000003
D.PW	= 000002	D.STATE	000006	D.UNIT	000005
EXIT	= 104411	I.ADDR	000006	I.FL	= 000000
I.TIME	000002	I.TYPE	000004	KP	= 000000
KEB	000060R	I.P	= 000004	WSTK	=0000005
WT	= 000002	W.DSA	= 000006	W.FLG	= 000003
W.FWA	= 000004	W.ICRT	= 000014	W.ICPM	000016
W.ICT	= 000010	W.NAM1	= 000022	W.NAM2	= 000024
W.DT	= 000012	W.PW	= 000026	W.PBNC	000027
W.BIH	= 000001	X.SUSP	000002	X.WAIT	000000
W.VDT	= 000020	PAGE.0	= 000000	PAGE.1	= 000001
PAGE.2	= 000002	PAGE.3	= 000003	PAGE.4	= 000004
PAGE.5	= 000005	PAGE.6	= 000006	PF	= 177000
PT	= 000006	P.AC0	= 000032	P.AC1	= 000042
P.AC2	= 000052	P.AC3	= 000062	P.AC4	= 000072
P.AC5	= 000102	P.REG	= 000002	P.FLG	= 000026
P.FPS	= 000030	P.PC	= 000020	P.DCF	= 000024
P.PSW	= 000022	P.P0	= 000004	P.P1	= 000006
P.P2	= 000010	P.P3	= 000012	P.P4	= 000014
P.P5	= 000016	REDKW	= 000000RG	R6	=00000006
P7	=0000007	SWP	= 177570	TASKSW	= 104410
TFOW	= 104412	TM	= 000003	WAITS	= 104404
.TRAP	= 104400				
.ANS.	000000				
	000100				

000

001

ERRORS DETECTED: 0

FREE CODE: 13401, WORDS

REDKW,LDI<SYN,REDKW,SRC

A-110

SYSMPS (MULTIPROCESSOR SYSTEM) MACPO V06-04A 17-AUG-77 01:09
TABLE OF CONTENTS

1- 2 SYMPS MULTIPROCESSOR OPERATING SYSTEM

SYMPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 17-AUG-77 01:09 PAGE 1

1 .TITLE SYMPS (MULTIPROCESSOR SYSTEM)
2 .SYTL SYMPS MULTIPROCESSOR OPERATING SYSTEM

SYSDS (MULTIPROCESSOR SYSTEM) MACRO 006-04A 17-AUG-77 01:09 PAGE 4
 SYSDS MULTIPROCESSOR OPERATING SYSTEM

```

1 1          : SUBROUTINE TO READ A CARD AND WAIT
2 2          MSTK = 05
3 3          :GLOBAL  REDCH
4 4          REDCH:
5 5          LDF (MSTK)+AC0      : CONVERT TO FIXED
6 6          STCF AC0-(MSTK)      ;
7 7          TST (MSTK)+
8 8          MOV (MSTK)+,RUPR      : ADDR OF BUFFER TO DFVR
9 9          LDF (MSTK)+AC0      : CONVERT TO FIXED
10 10         STCF AC0-(MSTK)      ;
11 11         TST (MSTK)+
12 12         MOV (MSTK)+,RCP      : BYTE COUNT TO DEVR
13 13         TST ICHK
14 14         RNF IFPR
15 15         RP FRST
16 16         :WORD 0
17 17         INITIO DFVR,IFPR
18 18         MOV #1,ICLK
19 19         01267
20 20         000001
21 21         17762
22 22         TFR:
23 23         15:
24 24         FRP:
25 25         00076
26 26         000207
27 27         00100
28 28         00102
29 29         00104
30 30         00105
31 31         00106
32 32         00110
33 33         00112
34 34         00114
35 35         00116
36 36         000000
37 37         .END

:FORWARD LINK
:DW, PAGE
:DEV, UNIT
:STATUS
:FUNCTION
:RUPR
:BYTE COUNT
:DDF

```

AC0	=000000	AC1	=000001	AC2	=000002
AC3	=000003	AC4	=000004	AC5	=000005
RCR	000112P	RURPR	000112P	RC0	=000001
R1	=000002	R10	=000000	R11	=000000
R12	=100000	R13	=000000	R14	=000000
R15	=100000	R2	=000004	R3	=000010
R4	=000020	R5	=000040	R6	=000100
R7	=000000	R8	=000000	R9	=000100
CP	=000000	CPVRP	000100P	DK	=000001
D.ACNT=	000014	D.RUPF=	000012	D.DPF	=000014
D.DEV	=000004	D.FL	=000000	D.FHUC	=000010
D.PAGE	=000003	D.DM	=000002	D.STJT=	000006
D.LIMIT=	000006	FRQ	000076P	FYJT	=104411
FRST	000034P	ICUK	000034P	FYPP	000052P
I.ADDR=	000006	T.FL	=000000	I.TYPP=	000002
I.TYPP=	000004	KP	=000000	IP	=000004
WSTK	=000005	MT	=000002	M.DSA	=000006
M.FLG	=000003	M.FWA	=000004	M.TCPT=	000014
M.TCPR=	000016	M.LGT	=000010	M.HBwi	=000022
M.NMAY=	000024	M.OPT	=000012	M.PV	=000026
M.PROC=	000027	M.PIH	=000001	M.SUSP=	000002
M.UAIT=	000000	M.YDT	=000020	PAGE.C=	000000
PAGE.1=	000001	PAGE.2=	000002	PAGE.3=	000003
PAGE.4=	000004	PAGE.5=	000005	PAGE.6=	000006
PP	=177000	PT	=000006	P.AC0	=000032
P.AC1	=000042	P.AC2	=000052	P.AC3	=000062
P.AC4	=000072	P.AC5	=000102	P.PFG	=000002
P.FLG	=000026	P.FPS	=000030	P.PC	=000020
P.PGE	=000024	P.DSM	=000022	P.P0	=000004
P.P1	=000004	P.Q2	=000010	P.P3	=000012
P.P4	=000014	P.P5	=000016	REDCN	=000000PG
P6	=000006	P7	=000007	SAP	=177570
TASKMS=	104010	TCRM	=104402	TW	=000003
TATTS=	104040	.TRAP	=104400		

• ARS.	000000	000
	000170	001

```
000720      001  
ERRORS DETECTED: 0  
FREE CORE: 13395. WORDS  
READCW,LP:<SYSYM,READCW,SRC
```

A-114

SJCR COMPTLF IMP45
DATE:-18-AUG-77
TIME:-00:10:30
SRIN JAVIAL


```

JUVIAL ISS                                     * HAPRIS JUVIAL CONDITLER
---VERSION -3A                                PAGE 1

'PROGRAM IMP45 *
'-----
'' IMP45 - INPUT PROCESSING FOR THE TOP 11/45 OF THIS ROUTINE
'' PERFORMS THE NECESSARY INITIALIZATION AND THEN ACCEPTS
'' COMMAND INPUTS FROM EITHER OF THE LSI-11'S OR THE IAS6.
'' THE DESIRED PROCESSING IS CARRIED OUT AND THE RESULTS ARE
'' RETURNED TO THE CALLING TERMINAL.
''
'' INPUTS:
'' LDDY = TABLE OF HANDSHAKE FLAGS BETWEEN LSI-11'S AND IAS
'' CRUF = TABLE OF COMMAND INPUT BUFFERS
'' DRUF = TABLE OF DATA INPUT BUFFERS
''
'' OUTPUTS:
'' OUTPUT RESULTS OF QUERY - EVENT OR REPORT TO CALLING LSI
''
'-----
'POUL INPUT SOURCES'
DO WHILE GO EQ 0 $
  IF LDDY(SOS) EQ 0 $
    THEN $
      CALL SRC45 $
    ELSE $
      END IF $
  IF LDDY (SIS) EQ 0 $ CALL L1SRC $
  IF LDDY (S2S) EQ 0 $ CALL L2SRC $
  END DO $
  'IGN WAS BEEN CANCELLED - EXIT & END'
  EXIT $
END SUBROUTINE $
SRC45 SUBROUTINE $
'-----
' THIS SUBROUTINE HANDLES QUERY PROCESSING FROM THE IAS6 KEYBOARD
' FIRST TRANSFER INPUT COMMAND TO RPN WORK BUFFER ICARD
' J = ACBUF(SOS) $
  TRANSFER ICARD,J $
  INSR = 0 $ 'DESIGNATE INPUT SOURCE'
  CALL CCNTL $ 'TRANSLATE & EXECUTE COMMAND'
  LDDY(SOS) = 1 $ 'FINISHED COMMAND'
  RETURN $
END SUBROUTINE $
L1SRC SUBROUTINE $
'-----
' THIS SUBROUTINE HANDLES QUERY PROCESSING FROM LSI NUMBER 1
' TRANSFER INPUT COMMAND TO RPN WORK BUFFER ICARD
' J = ACBUF(SIS) $
  TRANSFER ICARD,J $
  INSR = 1 $ 'DESIGNATE INPUT SOURCE'
  CALL CCNTL $ 'TRANSLATE & EXECUTE COMMAND'
  LDDY(SIS) = 1 $ 'SIGNAL FINISH'
  RETURN $
END SUBROUTINE $
L2SRC SUBROUTINE $
'-----
' THIS SUBROUTINE HANDLES QUERY PROCESSING FROM LSI NUMBER 2
' TRANSFER INPUT COMMAND TO RPN WORK BUFFER ICARD
' J = ACBUF(S2S) $
  TRANSFER ICARD,J $
  INSR = 2 $ 'DESIGNATE INPUT SOURCE'
  CALL CCNTL $ 'TRANSLATE AND EXECUTE COMMAND'
  LDDY(S2S) = 1 $ 'SIGNAL FINISH'

```

```

RETURN S
END SUBROUTINE S
DIRECT 4
MSTK = 55
-GLORI TRANC
LDF (MSTK)+,ACO
STCFI ACO,-(MSTK)
MOV R0,-(SP)
MOV R1,-(SP)
TST (MSTK)+
MOV (MSTK)+,R0
LDF (MSTK)+,ACO
STCFI ACO,-(MSTK)
TST (MSTK)+
MOV R0,R1
MOV (R0)+,a(MSTK)+
SR R1,R1
MOV (SP)+,R1
MOV (SP)+,R0
RTS PC
JOVIAL
END PROGRAM S

```

```

: CONVERT ADDR OF CRUF TO
: FIXED
: SAVE REG.
:
: ADDR OF CRUF IN R0
: CONVERT ADDR OF CARD
: TO FIXED
: R0 BYTES
: TRANSFER TO CARD
: RESTORE REG.

```

1s:

A-117

DATA BASE REFERENCE LISTING

S	5	13	0	0
CARD	0	2	1	40
INSDC	622	9	0	16
GN	623	9	0	16
LRDY	1653	9	0	16
CRUF	1667	9	0	16
J	2	13	0	16

COMPOOL SPACE USED = 1108

0 ERRORS

A-118

SPIN OPT
SPIN MACRO
MACRO V04-043
BRN,LPICSSVM,PMS,PPNML,MNSML,PPN,CDD,NSND

A-119

SYSDPS (MULTIPROCESSOR SYSTEM) MACRO V06-04A 18-AUG-77 00:13
TABLE OF CONTENTS

1- 2 SYSDPS MULTIPROCESSOR OPERATING SYSTEM
4- 3 PNMAC PM MACRO DEFINITIONS
4-125 PNMFO PROGRAM MODULE NUMBER EQUATES

SYSMPS (MULTIPROCESSOR SYSTEM) MICRO V06-04A 18-AUG-77 00:13 PAGE 1

1 .TITLE SYSMPS (MULTIPROCESSOR SYSTEM)
2 .SMTL SYSMPS MULTIPROCESSOR OPERATING SYSTEM

A-120

PWAC PM MACRO DEFINITIONS AND E MACRO V06-04A 18-AUG-77 00:13 PAGE 4
 PWAC PROGRAM MODULE NUMBERS FOLLOWS

```

127 000002 P4SKTR = 002.
128 000026 P11KTR = 022.
129 000052 P12KTR = 042.
130 000200 P10C = 128.
131 000201 P2SVIC = 120.
132 000202 P4SKTR = 130.
133 000203 P4C45 = 131.
134 000204 P4SSUM = 132.
135 000205 P4SCTR = 133.
136 000206 P4SS1 = 134.
137 000215 P1J0R1 = 141.
138 000216 P1J0R2 = 142.
139 000217 P1J0R3 = 143.
140 000220 P1J0R4 = 144.
141 000221 P1J0R5 = 145.
142 000222 P1J0R6 = 146.
143 000223 P1J0R7 = 147.
144 000224 P1K10 = 150.
145 000227 P1C11 = 151.
146 000230 P11SUM = 152.
147 000231 P11SA = 153.
148 000241 P1J0R1 = 161.
149 000242 P1J0R2 = 162.
150 000243 P1J0R3 = 163.
151 000244 P1J0R4 = 164.
152 000245 P1J0R5 = 165.
153 000252 P12KTR = 170.
154 000253 P1C12 = 171.
155 000254 P12SUM = 172.
156 000255 P12SR = 173.

: RESTORE NOT FUNCTION FOR 45
: RESTORE NOT FUNCTION FOR L1
: RESTORE NOT FUNCTION FOR L2
: 45 SYSTEM ERROR LOGGED
: COMMON SYSTEM ERROR LOGGED
: OVERLAY NOT FUNCTION FOR 45

:----
: INPUT PMS FOR
: BENCHMARK
:
:----
: OUTPUT ACT TABLE

: OVERLAY NOT FUNCTION FOR L1

:----
: OUTPUT PMS FOR
: BENCHMARK
:
:----
: OVERLAY NOT FUNCTION FOR L2

```

PWAC PW MACRO DEFINITIONS AND E MACRO V06-04A 1R-AUG-77 00:13 PAGE 5
 PWNEQ PROGRAM MODULE NUMBER EQUATES

.NLIST TTW
 .NLIST CND
 M.SET= 0

446
 447
 448 000000

PMWAC DU MACRO DEFINITIONS AND F MACRO V06-04A 18-AUG-77 00:13 PAGE 6
PMNEQ PROGRAM MODULE NUMBER EQUATES

```

1      .MACPD  REGIN ?X,?AI
2      .CLOPL  M$TAK
3
4      PSR      AI,?A,.FLPT
5      MOV      M$TAK,M$TK
6
7      FITNG
8      .FNDW
9      .MACPD  SFTUP X
10
11     .FNDW
12     .MACPD  STOP
13     .FNDW
14
15     ? CPDOL, ---- FOR ISS UNDFR MNS
16     .MACPD  CPDOL, A,A,C,?AI
17     .CLOPL  A
18     .CSFCT
19     .FNDW

```


[illegible]

PUMAC PW MACRO DEFINITIONS AND E MACRO V06-04A 19-AUG-77 00:13 PAGE 7-1
PUMAC DEGRAV MODULE MINIFR EQUATES

```

58 000334 012767 000002 000012G
59 000342 015704 000012G
60 000346 006304
61 000350 016401 003526G
62 000354 005000
63 000356
64 000366
65 000372
66
67 000372
68 000372
69 000376
70
71
72 000376 104411
73
74 000400
75
76 000424
77 000424
78 000424
79
80
81
82
83 000426
84 000426
85 000432
86 000434
87 000454
88
89 000462
90 000472
91 000512
92 000520
93
94 000524
95 000524
96
97 000550
98
99 000554
100 000554
101 000566
102 000600
103 000606
104
105 000620
106
107 000644
108
109 000670
110 000670
111 000670
112
113
114

MOV * 2,XREG00+<2*000005.>*000
YREG+<2*5>.R4
ASL R4
MOV COMP01+<2*000039.>(R4).R1
CLR R0
STND T1005
SLJ L2SPC
I1005: F01V *
END DO $
STMT 14
GOTO D101
T1001: F01V *
: 'IGN HAS BEEN CANCELLED - EXIT & END.'
EXIT $
EXIT ??
END SUBROUTINE $
PFTPN
SRC45 SUBROUTINE $
L03E9: F01V *
SRC45: F01V *
SETUP 0
: 'GLOBAL SRC45'
: 'THIS SUBROUTINE HANDLES QUERY PROCESSING FROM THE L336 KEYBOARD.'
: 'FIRST TRANSFER INPUT COMMAND TO RPN WORK BUFFER ICARD.'
J = ACPUF($06) $
STMT 20
MOV IC101 +<2*000000.>*000.-(MSTK)
CLR -(MSTK)
PUSHA 0,0,0,0,COMP01,00951,00,16 ;CRUF
POPI 2
TRANSC(CARD,J) $
F1TNG
PUSHA 0,0,0,0,COMP01,00000,01,40 ;CARD
PUSHJ 2
SJ TRANC
I1SPC = 0 $ 'DESIGNATE INPUT SOURCE'
STMT 22
MOVE 0,0,0,0,IC101,0,00,16,0,0,0,COMP01,00402,00,16 ;
CALL CCNTL $ 'TRANSLATE & EXECUTE COMMAND'
SLJ CCNTL
L03Y($06) = 1 $ 'FINISHED COMMAND'
STMT 24
PUSH 0,0,0,0,IC102,0,00,16
PUSHA 0,0,0,0,IC101,0,00,16
POPI 5
PUSHA 0,0,0,0,5,COMP01,00939,00,16 ;LRDY
PFTPN $
END SUBROUTINE $
PFTPN
L1SPC SUBROUTINE $
L03EA: F01V *
L1SPC: F01V *
SETUP 0
: 'GLOBAL L1SPC'
: 'THIS SUBROUTINE HANDLES QUERY PROCESSING FROM LST NUMBER 1.'
: 'TRANSFER INPUT COMMAND TO RPN WORK BUFFER ICARD'

```

```

115 000672      J = @CRUF($1$) S
116 000672      STMT 10
117 000672      PUSH 0,0,0,0,IC102,0,00,16
118 000704      PUSHA 0,0,0,0,COMPOL,00951,00,16 ;CRUF
119 000724      POPD 2
120 000724      TRANC(@CARD,J) S
121 000732      FLTNG
122 000742      PUSHA 0,0,0,0,COMPOL,00000,01,40 ;CARD
123 000762      PUSHT 2
124 000770      SJ TRANC
125 000774      INSPC = 1 S ;DESIGNATE INPUT SOURCE''
126 000774      STMT 32
127 000774      MOVF 0,0,0,0,IC102,0,00,16,0,0,0,0,COMPOL,00402,00,16 ;
128 000774      CALL CTRL S ;TRANSLATE & EXECUTE COMMAND''
129 001020      SJ CONTL
130 001020      LDY($1$) = 1 S ;SIGNAL FINISH''
131 001024      STMT 34
132 001024      PUSH 0,0,0,0,IC102,0,00,16
133 001036      PUSHA 0,0,0,0,IC102,0,00,16
134 001050      POPD 5
135 001056      POPP 0,0,0,0,5,COMPOL,00939,00,16 ;LRDY
136 001070      RETDPM S
137 001070      RETDPM
138 001070      FND SURROUTINE S
139 001114      RETDPM
140 001114      L2SPC SURROUTINE S
141 001140      L03ER: FOIV *
142 001140      L2SPC: FOIV *
143 001140      SETUP 0
144 001140      .CIRCUIT L2SPC
145 001140      ; THIS SURROUTINE HANDLES QUERY PROCESSING FROM LOT NUMBER 2''
146 001140      ; TRANSFER INPUT COMMAND TO PPN WPK BUFFER ICARD
147 001140      J = @CRUF($2$) S
148 001142      STMT 40
149 001142      PUSH 0,0,0,0,IC103,0,00,16
150 001154      PUSHA 0,0,0,0,COMPOL,00951,00,16 ;CRUF
151 001174      POPD 2
152 001174      TRANC(@CARD,J) S
153 001202      FLTNG
154 001212      PUSHA 0,0,0,0,COMPOL,00000,01,40 ;CARD
155 001232      PUSHT 2
156 001240      SJ TRANC
157 001244      INSPC = 2 S ;DESIGNATE INPUT SOURCE''
158 001244      STMT 42
159 001244      MOVF 0,0,0,0,IC103,0,00,16,0,0,0,0,COMPOL,00402,00,16 ;
160 001244      CALL CTRL S ;TRANSLATE AND EXECUTE COMMAND''
161 001270      SJ CONTL
162 001270      LDY($2$) = 1 S ;SIGNAL FINISH''
163 001274      STMT 44
164 001274      PUSH 0,0,0,0,IC102,0,00,16
165 001304      PUSHA 0,0,0,0,IC103,0,00,16
166 001320      POPD 5
167 001326      POPP 0,0,0,0,5,COMPOL,00939,00,16 ;LRDY
168 001340      RETDPM S
169 001340      RETDPM
170 001340      FND SURROUTINE S
171 001364      RETDPM

```


PMWAC PW MACRO DEFINITIONS AND F MACRO V06-04A 18-AUG-77 00:13 PAGE 7-3
PMWEO PROGRAM MODULE NUMBER EQUATES

Address	Operation	Comments
172	DIRECT \$	
173	MSTK = \$5	
174	MSTK = \$5	
175	CLARL TRANC	
176	CLARL TRANC	
177	TRANC: LDF	(MSTK)+,ACO
178	001410	172425
179	TRANC: LDF	(MSTK)+,ACO
180	001412	175445
181	STCFI	ACO,-(MSTK)
182	001414	010046
183	MNV	RO,-(SP)
184	001416	010146
185	MNV	RI,-(SP)
186	001420	005725
187	TST	(MSTK)+
188	001422	012500
189	MNV	(MSTK)+,RO
190	001424	172425
191	LDF	(MSTK)+,ACO
192	001426	175445
193	STCFI	ACO,-(MSTK)
194	001430	005725
195	TST	(MSTK)+
196	001432	012701 000120
197	MNV	RO,-PI
198	001436	
199	001436	012035
200	SNP	PI,18
201	001440	077102
202	001442	012601
203	001444	012600
204	RTS	PC
205	001446	000207
206	001450	
207	001450	
208	001450	
209	001450	
210	001450	
211	001450	
212	001450	
213	001450	
214	001452	
215	001464	
216	001465	
217	001470	
218	001470	

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PMWAC PW MACRO DEFINITIONS AND E MACRO V06-04A 18-AUG-77 00:13 PAGE 8
PMWEO PROGRAM MODULE NUMBER EQUATER

.END

000001

1

AC0	=000000	AC1	=0000001	AC2	=0000002	AC3	=0000003	AC4	=0000004
AC5	=0000005	AC6	=0000006	AC7	=0000007	AC8	=0000008	AC9	=0000009
AD0	=0000010	AD1	=0000011	AD2	=0000012	AD3	=0000013	AD4	=0000014
AD5	=0000015	AD6	=0000016	AD7	=0000017	AD8	=0000018	AD9	=0000019
AE0	=0000020	AE1	=0000021	AE2	=0000022	AE3	=0000023	AE4	=0000024
AE5	=0000025	AE6	=0000026	AE7	=0000027	AE8	=0000028	AE9	=0000029
AF0	=0000030	AF1	=0000031	AF2	=0000032	AF3	=0000033	AF4	=0000034
AF5	=0000035	AF6	=0000036	AF7	=0000037	AF8	=0000038	AF9	=0000039
AG0	=0000040	AG1	=0000041	AG2	=0000042	AG3	=0000043	AG4	=0000044
AG5	=0000045	AG6	=0000046	AG7	=0000047	AG8	=0000048	AG9	=0000049
AH0	=0000050	AH1	=0000051	AH2	=0000052	AH3	=0000053	AH4	=0000054
AH5	=0000055	AH6	=0000056	AH7	=0000057	AH8	=0000058	AH9	=0000059
AI0	=0000060	AI1	=0000061	AI2	=0000062	AI3	=0000063	AI4	=0000064
AI5	=0000065	AI6	=0000066	AI7	=0000067	AI8	=0000068	AI9	=0000069
AJ0	=0000070	AJ1	=0000071	AJ2	=0000072	AJ3	=0000073	AJ4	=0000074
AJ5	=0000075	AJ6	=0000076	AJ7	=0000077	AJ8	=0000078	AJ9	=0000079
AK0	=0000080	AK1	=0000081	AK2	=0000082	AK3	=0000083	AK4	=0000084
AK5	=0000085	AK6	=0000086	AK7	=0000087	AK8	=0000088	AK9	=0000089
AL0	=0000090	AL1	=0000091	AL2	=0000092	AL3	=0000093	AL4	=0000094
AL5	=0000095	AL6	=0000096	AL7	=0000097	AL8	=0000098	AL9	=0000099
AM0	=0000100	AM1	=0000101	AM2	=0000102	AM3	=0000103	AM4	=0000104
AM5	=0000105	AM6	=0000106	AM7	=0000107	AM8	=0000108	AM9	=0000109
AN0	=0000110	AN1	=0000111	AN2	=0000112	AN3	=0000113	AN4	=0000114
AN5	=0000115	AN6	=0000116	AN7	=0000117	AN8	=0000118	AN9	=0000119
AO0	=0000120	AO1	=0000121	AO2	=0000122	AO3	=0000123	AO4	=0000124
AO5	=0000125	AO6	=0000126	AO7	=0000127	AO8	=0000128	AO9	=0000129
AP0	=0000130	AP1	=0000131	AP2	=0000132	AP3	=0000133	AP4	=0000134
AP5	=0000135	AP6	=0000136	AP7	=0000137	AP8	=0000138	AP9	=0000139
AQ0	=0000140	AQ1	=0000141	AQ2	=0000142	AQ3	=0000143	AQ4	=0000144
AQ5	=0000145	AQ6	=0000146	AQ7	=0000147	AQ8	=0000148	AQ9	=0000149
AR0	=0000150	AR1	=0000151	AR2	=0000152	AR3	=0000153	AR4	=0000154
AR5	=0000155	AR6	=0000156	AR7	=0000157	AR8	=0000158	AR9	=0000159
AS0	=0000160	AS1	=0000161	AS2	=0000162	AS3	=0000163	AS4	=0000164
AS5	=0000165	AS6	=0000166	AS7	=0000167	AS8	=0000168	AS9	=0000169
AT0	=0000170	AT1	=0000171	AT2	=0000172	AT3	=0000173	AT4	=0000174
AT5	=0000175	AT6	=0000176	AT7	=0000177	AT8	=0000178	AT9	=0000179
AV0	=0000180	AV1	=0000181	AV2	=0000182	AV3	=0000183	AV4	=0000184
AV5	=0000185	AV6	=0000186	AV7	=0000187	AV8	=0000188	AV9	=0000189
AW0	=0000190	AW1	=0000191	AW2	=0000192	AW3	=0000193	AW4	=0000194
AW5	=0000195	AW6	=0000196	AW7	=0000197	AW8	=0000198	AW9	=0000199
AX0	=0000200	AX1	=0000201	AX2	=0000202	AX3	=0000203	AX4	=0000

```

* TRAP - 000000 000
* APS. 000000 000
          001470 001
ERRORS DETECTED: 1
ERRORS DETECTED: 1
FREE CODE: 0070. 00000
PPN.TP:SSYSYM.PVS.00000

```

FREE COPY: 8070. WARD'S

A-130

SPATISH
TIME:00:15:18

A-131

SJCH CNDTIF OK SUBS
DATE:-17-AUG-77
TIME:-00:11:01
SDUN PTP
PTD VIC-03A
SDPW.SAC/DE
SCOMPOL.001/DE
SCOMPOL.001CNDPOL.ISS
SDPW.SAC/CI/FA
SEND
SDUN JOWIAL

JUVIAL ISS
PAGE 3

* HAPOTS JUVIAL COMPTIER
---VERSION -3A

PAGE 1 1

A-132


```

JUVIAL ISS                                *  HADNIS JUVIAL COMPILER  PAGE 2
POLISH SUBROUTINE  *
-----
POLISH GENERATOR - ACCEPTS OPERATORS/OPERANDS FROM A SOURCE
STRING AND BUILDS A REVERSE POLISH TARGET STRING
INPUTS ARE:
  INTYP = 0 = OPERAND (DATA POINTER)
  1 = OPERATOR (KEYWORD NUMBER)
  2 = OPERAND (CONSTANT POINTER)
  3 = END OF SOURCE STRING
  4 = DATA CONSTANT
TTDTR = TARGETABLE POINTER FOR COMPOUND DATA
TKYND = KEYWORD NUMBER OF OPERATOR
COTR = TARGETABLE POINTER FOR CONSTANT
OUTPUTS ARE:
  OPSTK = A MODIFIED POLISH TARGET STACK (ACCESSED BY PNTRY
(PINDX) )
  OPSTV = A MODIFIED OPERATOR STACK (ACCESSED BY OPDTR
(OPNDX) )
-----
CASE INTYP *
  OF 0 *
    CALL OPDND *
    " 0 MEANS OPERAND "
  OF 1 *
    CALL OPDTR *
    " 1 MEANS OPERATOR "
  OF 2 *
    CALL CONST *
    " OPERAND/CONSTANT "
  OF 3 *
    CALL FINSH *
    " END OF COMMAND "
  OF 4 *
    CALL STRNC *
    " DATA CONSTANT CHAP "
END CASE *
END CASE *
RETURN *
END SUBROUTINE *

OPDND SUBROUTINE *
  PNTRY(OPNDX) = TTPTR *
  PINDX = PINDX + 1 *
  RETURN *
END SUBROUTINE *

OPDTR SUBROUTINE *
  IF OPNDX EQ 0 *
    THEN *
      " 0 MEANS TOP OF OPERATOR STACK "
      " PUT KEYWORD ON OPSTK "
      OPDTR(OPNDX) = TKYND *
      OPNDX = OPNDX + 1 *
      OPDTR(OPNDX) = FESCHR *
      OPNDX = OPNDX + 1 *
      ELSE *
        " COMPARE HIERARCHY "
        TI = OPDTR(OPNDX - 2) *

```

```

JOVIAL ISS
* HARRIS JOVIAL COMPILER
---VERSION -3A
PAGE 3

TJ = 0 S
DO WHILE TJ EQ 0 S
  IF KYHIV(STRYMS) I/O KYHIV(STIS) S
    THEN S
      OPNDX = OPNDX - 1 S
      PNTRY(SPINDXS) = OPPTP(SOPNDXS) S
      PINDX = PINDX + 1 S
      OPNDX = OPNDX - 1 S
      PNTRY(SPINDXS) = OPPTP(SOPNDXS) S
      PINDX = PINDX + 1 S
      ELSE S
        TJ = 1 S
      END IF S
    IF OPNDX EQ 0 S TJ = 1 S
    TT = OPPTP(SOPNDX - 2S) S
  END DO S
  OPPTP(SOPNDXS) = TKYNM S
  OPNDX = OPNDX + 1 S
  OPPTP(SOPNDXS) = ESCHR S
  OPNDX = OPNDX + 1 S
  END IF S
  RETURN S
END SUBROUTINE S

CONST SUBROUTINE S
  PNTRY(SPINDXS) = ATCHR S
  PINDX = PINDX + 1 S
  PNTRY(SPINDXS) = CPTP S
  PINDX = PINDX + 1 S
  RETURN S
END SUBROUTINE S

FINSH SUBROUTINE S
  DO UNTIL OPNDX EQ 0 S
    OPNDX = OPNDX - 1 S
    PNTRY(SPINDXS) = OPPTP(SOPNDXS) S
    PINDX = PINDX + 1 S
  END DO S
  RETURN S
END SUBROUTINE S

STRNG SUBROUTINE S
  PNTRY(SPINDXS) = SLASH S
  PINDX = PINDX + 1 S
  PNTRY(SPINDXS) = TTPTP S
  PINDX = PINDX + 1 S
  RETURN S
END SUBROUTINE S
PAGE S

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```

JOVIAL ISS                                *  HARRIS JOVIAL COMPILER  PAGE. 6
---VERSTON -3A

COCNV SUBROUTINE S
COCNV - CHECKS A STRING TO SEE IF IT IS A DECIMAL STRING AND IF
SO, CONVERTS IT TO A DECIMAL BINARY NUMBER
INPUTS ARE:
TCARD = TABLE CONTAINING THE COMMAND LINE
ICOL = INDEX TO INPUT CHARACTER STRING TCARD
ISLEN = LENGTH OF INPUT CHARACTER STRING (BYTES)
OUTPUTS ARE:
CVAL = CONVERTED RESULT - EQUIVALENCED TO TAGTABLE
DCR = 0 = NOT A DECIMAL CONSTANT
      1 = DENOTES DECIMAL CONSTANT
CPTR = STORE INDEX IN TAGTABLE OF CVAL.
-----
DCR = 1 S
SUM = 0 S
I = 0 S
DO UNTIL I GO ISLEN S
  J = 0 S
  DO WHILE J IS 10 S
    IF TCARD(ICOLS) EQ IDEC(SJS) S
      THEN S
      SUM = SUM * 10 + J S " NEW SUM "
      ICOL = ICOL + 1 S " STEP INDEX "
      J = 10 S " END DO "
    ELSE S
      J = J + 1 S
    IF J EQ 10 S DCR = 0 S
  END IF S
  I = I + 1 S
END DO S
IF DCR EQ 1 S
  THEN S
    CVAL(STIDTPS) = SUM S " STORE CONSTANT IN TAGTBL "
    CPTR = TTPTP S " SAVE INDEX "
    TTPTP = TTPTP + 1 S
  ELSE S
    END IF S
  RETURN S
END SUBROUTINE S
END PROGRAM S

```

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DATA BASE REFERENCE LISTING

S	5	13	0	0	0
ICARD	74	14	0	0	0
FSCHR	74	9	0	0	0
SLASH	74	9	0	0	0
ATCHR	75	9	0	0	0
INDEC	67	14	0	0	0
ICOL	104	9	0	0	0
SHM	115	9	0	0	0
TEPR	120	9	0	0	0
NTAG	122	9	0	0	0
A	124	9	0	0	0
R	125	9	0	0	0
C	126	9	0	0	0
D	127	9	0	0	0
TAC	170	14	0	0	0
KVPTA	226	9	0	0	0
KYHUN	244	9	0	0	0
KYHIY	322	9	0	0	0
KYIEN	360	9	0	0	0
KOP	416	14	0	0	0
KMENT	562	9	0	0	0
ISLEN	563	9	0	0	0
OPNDX	564	9	0	0	0
ICTYP	565	9	0	0	0
PLNDX	566	9	0	0	0
TYNVM	567	9	0	0	0
TPPTR	570	9	0	0	0
INTYP	571	9	0	0	0
OCF	573	9	0	0	0
CPTA	574	9	0	0	0
TJ	604	9	0	0	0
TJ	605	9	0	0	0
TFPR	620	9	0	0	0
NPTR	670	14	0	0	0
PUTRY	740	14	0	0	0
TTYP	1060	9	0	0	0
TFA	1104	9	0	0	0
TNR	1130	9	0	0	0
TADDR	1154	9	0	0	0
CVAL	1060	10	0	0	0
I	1	13	0	0	0
J	2	13	0	0	0
K	3	13	0	0	0
L	4	13	0	0	0
M	5	13	0	0	0

COMPOUL SPACE USED = 1134

0 ERRORS

A-139

SPINISH
TIME:-00:17:35

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RADC plans and conducts research, exploratory and advanced development programs in command, control, and communications (C³) activities, and in the C³ areas of information sciences and intelligence. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

